MST91A4Q1
FHD LCD Controller with High Frame Rate

Preliminary Data Sheet Version 0.1

REVISION HISTORY

Revision No.	Description	Date
0.1	Ÿ Initial release	07/25/2018

Doc. No. : 2018070594

FEATURES

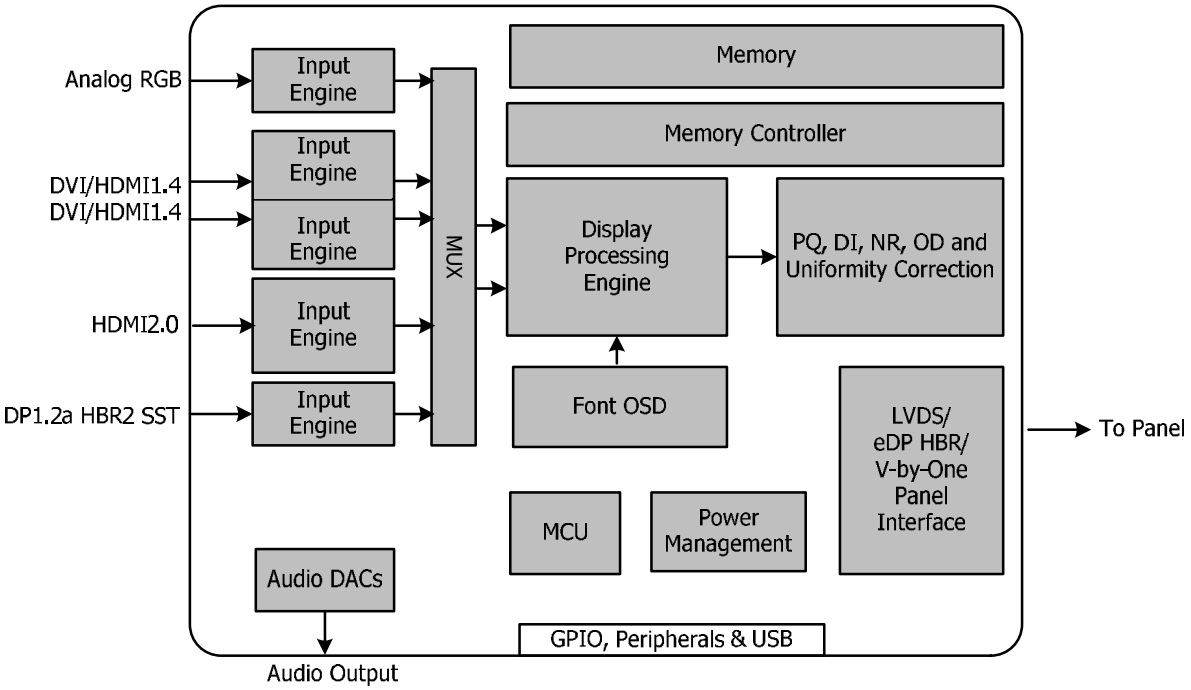
MST91A4Q1 key features include:

1. *High-quality scaling engine supports up to FHD (1920x1080) @144Hz Panel*
2. *Multi-function digital interface engines*
3. *Integrated single links or dual-link DVI compliant receivers*
4. *Integrated HDMI2.0 compliant receiver*
5. *Integrated DP1.2a SST compliant receiver*
6. *10-bit data processing and programmable 12-bit gamma for R, G, B (CLUT)*
7. *Built-in LVDS/ eDP HBR/ V-by-One transmitter*
8. *EPLQFP package*

- Analog RGB Compliant Input Ports
  - One analog port supports up to 205MHz (up to UXGA @75Hz)
  - On-chip high-performance PLLs (only a single reference crystal required)
  - Supports composite Sync and SOG (Sync-on-Green) separator
- Auto-Configuration/Auto-Detection
  - Auto input signal format (SOG, Composite, Separated HSYNC, VSYNC, and DE), and input mode (all VESA & IBM modes w/ resolution and polarity) detection
  - Auto-tuning function including phasing, positioning, offset, gain, and jitter detection
  - Sync Detection for H/V Sync
- Configurable Compliant Input Ports
  - Four Input Digital Ports
  - Two single-link or one dual-link DVI/HDMI1.4 Compliant Input Ports
  - One HDMI2.0 Compliant Input Port
  - One DP1.2a HBR2 Compliant Input Port
  - Supports HDMI CEC ports
  - DVI operates up to 165MHz (up to UXGA @60Hz)
  - Single link or dual-link on-chip DVI 1.0 compliant receiver
  - Supports HDMI2.0 8/10/12-bit deep color mode
  - Supports HDMI2.0 input resolution up to 1920x1080@144Hz
  - Display Port v1.2a compliant receivers supports HBR2 and SST with resolution up to 1920x1080@144Hz
  - High-bandwidth Digital Content Protection (HDCP) 2.2 compliant receiver over HDMI2.0
- DisplayPort
  - DisplayPort v1.2a compliant
  - Supports 5.4Gbps, 2.7Gbps and 1.62Gbps per lane, receiver offering 21.6Gbps bandwidth over 4 lanes
  - Bi-directional auxiliary channel to flexibly deliver control and status information
  - Embedded clock architecture to reduce electromagnetic interference (EMI) susceptibility and physical wire count
  - Supports High-bandwidth Digital Content Protection (HDCP) v1.3 to protect the transmission of AV content
  - Supports hot plug/unplug detection and link status failure detection
  - 2-channel L-PCM and IEC 61937 compressed formats
- High-Performance Scaling and PQ Engine
  - Fully Programmable shrink/zoom capabilities
  - 10-bit data processing
  - Support automatic 3:2 pull-down & 2:2 pull-down detection and recovery
  - Supports 3D-adaptive video de-interlace and noise reduction
  - Supports sRGB and xvYCC color processing
  - Supports HDMI1.4/2.0 and DP1.2a deep color formats
  - Supports 17x17x17 3D LUT
  - Programmable 12-bit RGB gamma CLUT
  - Sharpness enhancement and color control
- Frame Buffer Support
  - Frame rate conversion
  - Embedded frame buffer

- Response Time Enhancement
  - Programmable look-up table with various word-length selections
  - Proprietary algorithm for memory size reduction
  - Programmable RTE strength
- Output Display Interface
  - Supports up to 1920x1080@144Hz panel interface
  - Supports 4-ch LVDS interfaces
  - Supports eDP compliant transmitter up to 4 lanes with 2.7Gbps link rate
  - Supports 8 pairs Vx1@3Gbps interface
  - Supports flexible spread spectrum frequency and up modulation
- Analog Audio Interface
  - Stereo L/R line input & output
  - Built-in audio output DAC
  - Separates ADC for L/R channel
  - Digital PGA control range from -112dB to +12dB with fading and mute function
- Digital Audio Interface
  - Supports master I2S output interface for digital audio
  - Supports mute and fading function
- Fonts On-screen Display Controller (OSD)
  - One OSD generator with 2048 character font programmable RAM
  - OSD programmable font height
  - Supports 2/4/8 multi-color fonts
  - Supports 512 color palette
  - Supports 6K code attributes
  - Gradient color function
  - Pattern generator for production test
  - Supports OSD MUX and alpha blending capability
  - Supports OSD gradient engine
- Super Resolution and Uniformity Correction
  - Supports MStar latest UCE (Ultra-Clear-Engine) with super resolution technology up to 1920x1080
  - Uniformity correction supports horizontal and vertical sampling unit is 64x64 (max)
  - Uniformity correction supports R, G, B setup independently and five layers (0, 64, 128, 192, 256).
- Integrated Micro Controller
  - Embedded one 8032 and one powerful 32-bit micro controllers
  - Configurable PWMs and GPIOs
  - SPI bus for external flash

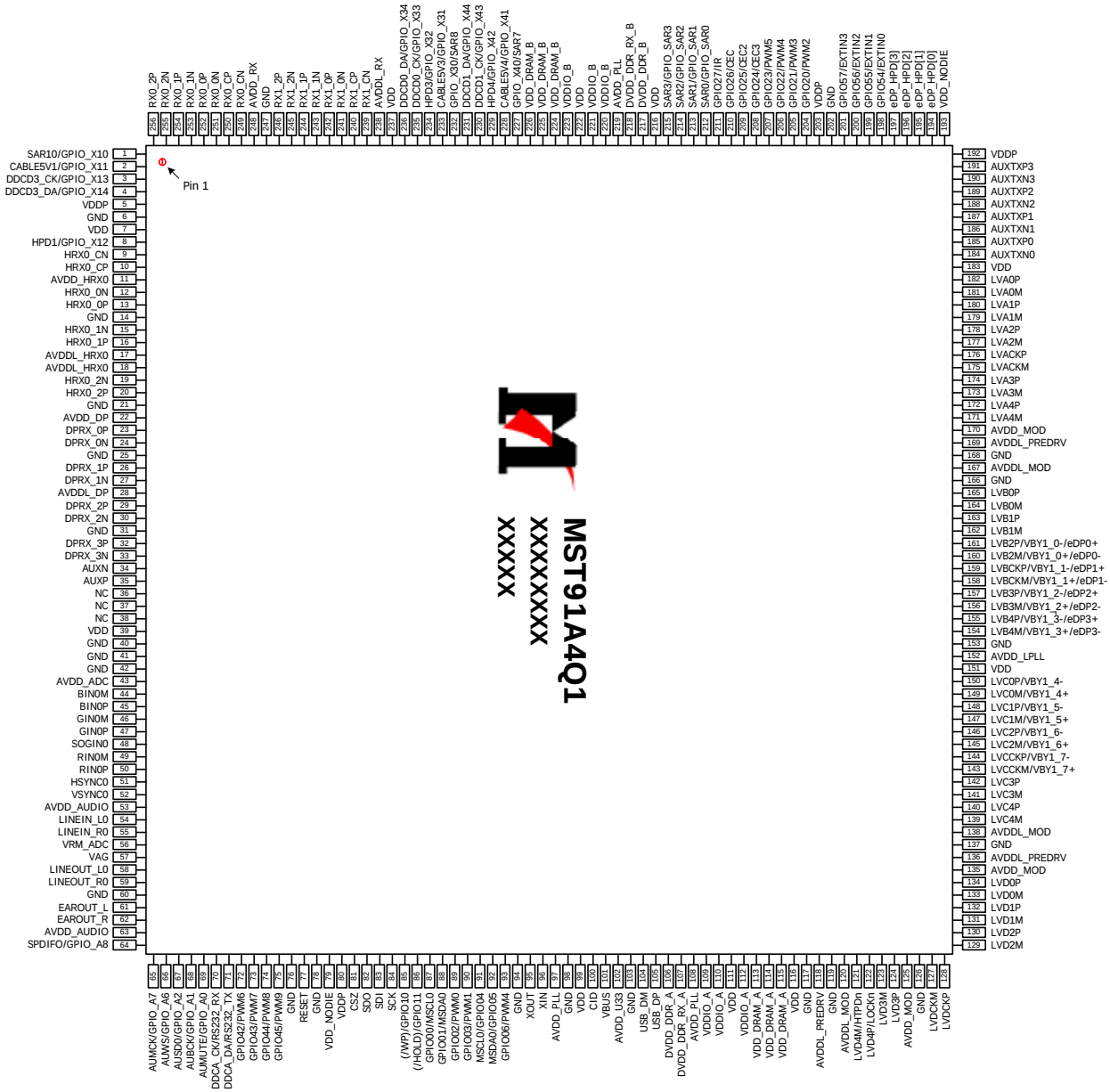
BLOCK DIAGRAM



GENERAL DESCRIPTION

The MST91A4Q1 is MStar latest total SoC solution processing IC for the latest state-of-the-art stereo display LCD monitors with panel resolutions up to FHD (1920x1080)@144Hz. It is configured with an integrated ADC/PLL, integrated multi-function DVI/HDMI2.0/DP1.2a receivers as configurable digital inputs, a high quality 10-bit processing display processing engine, and RTE engine for response-time enhancement. It equipped new, low wire count, low EMI video interface, Embedded DisplayPort (eDP) with 2.7Gbps link rate and V-by-One and LVDS interface technology. The MST91A4Q1 supports complete interoperability-providing DisplayPort1.2a interface with 5.4Gbps/lane. To further reduce system costs, the MST91A4Q1 also integrates intelligent power management control capability for green-mode requirements and spread-spectrum support for EMI management.

PIN DIAGRAM (MST91A4Q1)



PIN DESCRIPTION

Analog Interface

Pin Name	Pin Type	Function	Pin
BIN0M	Analog Input	Reference Ground for Analog Blue Input	44
BIN0P	Analog Input	Analog Blue Input	45
GIN0M	Analog Input	Reference Ground for Analog Green Input	46
GIN0P	Analog Input	Analog Green Input	47
RIN0M	Analog Input	Reference Ground for Analog Red Input	49
RIN0P	Analog Input	Analog Red Input	50
SOGIN0	Analog Input	Sync-On-Green Input	48
HSYNC0	Schmitt Trigger Input w/ 5V-tolerant	Analog HSYNC Input	51
VSYNC0	Schmitt Trigger Input w/ 5V-tolerant	Analog VSYNC Input	52

Analog Audio Interface

Pin Name	Pin Type	Function	Pin
EAROUT_L	Analog Output	Audio Left Channel Headphone Output	61
EAROUT_R	Analog Output	Audio Right Channel Headphone Output	62
LINEIN_L0	Analog Input	Main Audio Line Input Left 0 Channel	54
LINEIN_R0	Analog Input	Main Audio Line Input Right 0 Channel	55
LINEOUT_L0	Analog Output	Main Audio Line Output Left 0 Channel (needs external RC filter)	58
LINEOUT_R0	Analog Output	Main Audio Line Output Right 0 Channel (needs external RC filter)	59
VAG	Analog Output	Reference Voltage for Audio Common Mode	57
VRM_ADC	Analog Output	Negative Reference Voltage for Audio ADC	56

Digital Audio Interface

Pin Name	Pin Type	Function	Pin
GPIO_A0/ AUMUTE	I/O w/5V-tolerant/ Output	General Purpose Input/Output; 4mA driving strength/ Audio Output Mute control	69
GPIO_A1/ AUBCK	I/O w/5V-tolerant/ Output	General Purpose Input/Output; 4mA driving strength/ Audio Bit Clock Output	68
GPIO_A2/ AUSD0	I/O w/5V-tolerant/ Output	General Purpose Input/Output; 4mA driving strength/ Audio Serial Data0 Output	67
GPIO_A6/ AUWS	I/O w/5V-tolerant/ Output	General Purpose Input/Output; 4mA driving strength/ Audio Serial Word Select Output	66
GPIO_A7/ AUMCK	I/O w/5V-tolerant/ Output	General Purpose Input/Output; 4/8mA driving strength/ Audio Master Clock Output	65
GPIO_A8/ SPDIFO	I/O w/5V-tolerant/ Output	General Purpose Input/Output; 4/8mA driving strength/ Digital Audio Output	64

Digital Input Ports Interface

Pin Name	Pin Type	Function	Pin
DP_RX0N	Input	DP SST Main-Link Lane 0 Negative Signal Input	24
DP_RX0P	Input	DP SST Main-Link Lane 0 Positive Signal Input	23
DP_RX1N	Input	DP SST Main-Link Lane 1 Negative Signal Input	27
DP_RX1P	Input	DP SST Main-Link Lane 1 Positive Signal Input	26
DP_RX2N	Input	DP SST Main-Link Lane 2 Negative Signal Input	30
DP_RX2P	Input	DP SST Main-Link Lane 2 Positive Signal Input	29
DP_RX3N	Input	DP SST Main-Link Lane 3 Negative Signal Input	33
DP_RX3P	Input	DP SST Main-Link Lane 3 Positive Signal Input	32
HRX0_0N	Input	High-speed HDMI Main-Link 0 Lane 0 Negative Signal Input	12
HRX0_0P	Input	High-speed HDMI Main-Link 0 Lane 0 Positive Signal Input	13
HRX0_1N	Input	High-speed HDMI Main-Link 0 Lane 1 Negative Signal Input	15
HRX0_1P	Input	High-speed HDMI Main-Link 0 Lane 1 Positive Signal Input	16
HRX0_2N	Input	High-speed HDMI Main-Link 0 Lane 2 Negative Signal Input	19
HRX0_2P	Input	High-speed HDMI Main-Link 0 Lane 2 Positive Signal Input	20
HRX0_CN	Input	High-speed HDMI Main-Link 0 Negative Clock Channel	9
HRX0_CP	Input	High-speed HDMI Main-Link 0 Positive Clock Channel	10
RX0_0N	Input	DVI/HDMI Main-Link 0 Lane 0 Negative Signal Input	251
RX0_0P	Input	DVI/HDMI Main-Link 0 Lane 0 Positive Signal Input	252
RX0_1N	Input	DVI/HDMI Main-Link 0 Lane 1 Negative Signal Input	253
RX0_1P	Input	DVI/HDMI Main-Link 0 Lane 1 Positive Signal Input	254

Pin Name	Pin Type	Function	Pin
RX0_2N	Input	DVI/HDMI Main-Link 0 Lane 2 Negative Signal Input	255
RX0_2P	Input	DVI/HDMI Main-Link 0 Lane 2 Positive Signal Input	256
RX0_CN	Input	DVI/HDMI Main-Link 0 Negative Clock Channel	249
RX0_CP	Input	DVI/HDMI Main-Link 0 Positive Clock Channel	250
RX1_0N	Input	DVI/HDMI Main-Link 1 Lane 0 Negative Signal Input	241
RX1_0P	Input	DVI/HDMI Main-Link 1 Lane 0 Positive Signal Input	242
RX1_1N	Input	DVI/HDMI Main-Link 1 Lane 1 Negative Signal Input	243
RX1_1P	Input	DVI/HDMI Main-Link 1 Lane 1 Positive Signal Input	244
RX1_2N	Input	DVI/HDMI Main-Link 1 Lane 2 Negative Signal Input	245
RX1_2P	Input	DVI/HDMI Main-Link 1 Lane 2 Positive Signal Input	246
RX1_CN	Input	DVI/HDMI Main-Link 1 Negative Clock Channel	239
RX1_CP	Input	DVI/HDMI Main-Link 1 Positive Clock Channel	240

LVDS Interface

Pin Name	Pin Type	Function	Pin
LVA0M	Output	LVDS A-Link Channel 0 Negative Data Output	181
LVA0P	Output	LVDS A-Link Channel 0 Positive Data Output	182
LVA1M	Output	LVDS A-Link Channel 1 Negative Data Output	179
LVA1P	Output	LVDS A-Link Channel 1 Positive Data Output	180
LVA2M	Output	LVDS A-Link Channel 2 Negative Data Output	177
LVA2P	Output	LVDS A-Link Channel 2 Positive Data Output	178
LVA3M	Output	LVDS A-Link Channel 3 Negative Data Output	173
LVA3P	Output	LVDS A-Link Channel 3 Positive Data Output	174
LVA4M	Output	LVDS A-Link Channel 4 Negative Data Output	171
LVA4P	Output	LVDS A-Link Channel 4 Positive Data Output	172
LVACKM	Output	LVDS A-Link Negative Clock Output	175
LVACKP	Output	LVDS A-Link Positive Clock Output	176
LVB0M	Output	LVDS B-Link Channel 0 Negative Data Output	164
LVB0P	Output	LVDS B-Link Channel 0 Positive Data Output	165
LVB1M	Output	LVDS B-Link Channel 1 Negative Data Output	162
LVB1P	Output	LVDS B-Link Channel 1 Positive Data Output	163
LVB2M	Output	LVDS B-Link Channel 2 Negative Data Output	160
LVB2P	Output	LVDS B-Link Channel 2 Positive Data Output	161
LVB3M	Output	LVDS B-Link Channel 3 Negative Data Output	156
LVB3P	Output	LVDS B-Link Channel 3 Positive Data Output	157
LVB4M	Output	LVDS B-Link Channel 4 Negative Data Output	154
LVB4P	Output	LVDS B-Link Channel 4 Positive Data Output	155
LVBCKM	Output	LVDS B-Link Negative Clock Output	158

Pin Name	Pin Type	Function	Pin
LVBCKP	Output	LVDS B-Link Positive Clock Output	159
LVC0M	Output	LVDS C-Link Channel 0 Negative Data Output	149
LVC0P	Output	LVDS C-Link Channel 0 Positive Data Output	150
LVC1M	Output	LVDS C-Link Channel 1 Negative Data Output	147
LVC1P	Output	LVDS C-Link Channel 1 Positive Data Output	148
LVC2M	Output	LVDS C-Link Channel 2 Negative Data Output	145
LVC2P	Output	LVDS C-Link Channel 2 Positive Data Output	146
LVC3M	Output	LVDS C-Link Channel 3 Negative Data Output	141
LVC3P	Output	LVDS C-Link Channel 3 Positive Data Output	142
LVC4M	Output	LVDS C-Link Channel 4 Negative Data Output	139
LVC4P	Output	LVDS C-Link Channel 4 Positive Data Output	140
LVCCKM	Output	LVDS C-Link Negative Clock Output	143
LVCCKP	Output	LVDS C-Link Positive Clock Output	144
LVD0M	Output	LVDS D-Link Channel 0 Negative Data Output	133
LVD0P	Output	LVDS D-Link Channel 0 Positive Data Output	134
LVD1M	Output	LVDS D-Link Channel 1 Negative Data Output	131
LVD1P	Output	LVDS D-Link Channel 1 Positive Data Output	132
LVD2M	Output	LVDS D-Link Channel 2 Negative Data Output	129
LVD2P	Output	LVDS D-Link Channel 2 Positive Data Output	130
LVD3M	Output	LVDS D-Link Channel 3 Negative Data Output	123
LVD3P	Output	LVDS D-Link Channel 3 Positive Data Output	124
LVD4M	Output	LVDS D-Link Channel 4 Negative Data Output	121
LVD4P	Output	LVDS D-Link Channel 4 Positive Data Output	122
LVDCKM	Output	LVDS D-Link Negative Clock Output	127
LVDCKP	Output	LVDS D-Link Positive Clock Output	128

V-by-One Interface

Pin Name	Pin Type	Function	Pin
VBY1_0-	Output	VBY1 Channel 0 Negative Data Output	161
VBY1_0+	Output	VBY1 Channel 0 Positive Data Output	160
VBY1_1-	Output	VBY1 Channel 1 Negative Data Output	159
VBY1_1+	Output	VBY1 Channel 1 Positive Data Output	158
VBY1_2-	Output	VBY1 Channel 2 Negative Data Output	157
VBY1_2+	Output	VBY1 Channel 2 Positive Data Output	156
VBY1_3-	Output	VBY1 Channel 3 Negative Data Output	155
VBY1_3+	Output	VBY1 Channel 3 Positive Data Output	154

Pin Name	Pin Type	Function	Pin
VBY1_4-	Output	VBY1 Channel 4 Negative Data Output	150
VBY1_4+	Output	VBY1 Channel 4 Positive Data Output	149
VBY1_5-	Output	VBY1 Channel 5 Negative Data Output	148
VBY1_5+	Output	VBY1 Channel 5 Positive Data Output	147
VBY1_6-	Output	VBY1 Channel 6 Negative Data Output	146
VBY1_6+	Output	VBY1 Channel 6 Positive Data Output	145
VBY1_7-	Output	VBY1 Channel 7 Negative Data Output	144
VBY1_7+	Output	VBY1 Channel 7 Positive Data Output	143
HTPDn	I/O	VBY1 Video Hot Plug Detection Output	121
LOCKn	I/O	VBY1 Video Lock Detection Output	122

eDP Interface

Pin Name	Pin Type	Function	Pin
eDP0-	Output	eDP Channel 0 Negative Data Output	160
eDP0+	Output	eDP Channel 0 Positive Data Output	161
eDP1-	Output	eDP Channel 1 Negative Data Output	158
eDP1+	Output	eDP Channel 1 Positive Data Output	159
eDP2-	Output	eDP Channel 2 Negative Data Output	156
eDP2+	Output	eDP Channel 2 Positive Data Output	157
eDP3-	Output	eDP Channel 3 Negative Data Output	154
eDP3+	Output	eDP Channel 3 Positive Data Output	155

eDP TX AUX & HPD Interface

Pin Name	Pin Type	Function	Pin
AUXTXN0	Input / Output	eDP TX AUX0 Negative Data Output (HPD pin needs using eDP_HPD[0] correspondingly)	184
AUXTXN1	Input / Output	eDP TX AUX1 Negative Data Output (HPD pin needs using eDP_HPD[1] correspondingly)	186
AUXTXN2	Input / Output	eDP TX AUX2 Negative Data Output (HPD pin needs using eDP_HPD[2] correspondingly)	188
AUXTXN3	Input / Output	eDP TX AUX3 Negative Data Output (HPD pin needs using eDP_HPD[3] correspondingly)	190
AUXTXP0	Input / Output	eDP TX AUX0 Positive Data Output (HPD pin needs using eDP_HPD[0] correspondingly)	185
AUXTXP1	Input / Output	eDP TX AUX1 Positive Data Output (HPD pin needs using eDP_HPD[1] correspondingly)	187
AUXTXP2	Input / Output	eDP TX AUX2 Positive Data Output (HPD pin needs using eDP_HPD[2] correspondingly)	189
AUXTXP3	Input / Output	eDP TX AUX3 Positive Data Output (HPD pin needs using eDP_HPD[3] correspondingly)	191
eDP_HPD[0]	Input	eDP HPD signal [3:0] bit0	194
eDP_HPD[1]	Input	eDP HPD signal [3:0] bit1	195
eDP_HPD[2]	Input	eDP HPD signal [3:0] bit2	196
eDP_HPD[3]	Input	eDP HPD signal [3:0] bit3	197

GPIO Interface

Pin Name	Pin Type	Function	Pin
GPIO00/ MSCL0	I/O w/5V-tolerant	General Purpose Input/Output; 4mA driving strength / Master I2C Clock	87
GPIO01/ MSDA0	I/O w/5V-tolerant	General Purpose Input/Output; 4mA driving strength / Master I2C Data	88
GPIO02/ PWM0/ RS232_TX	I/O w/5V-tolerant/ Output/ I/O w/ 5V-tolerant	General Purpose Input/Output; 4mA driving strength/ Pulse Width Modulation Output/ UART Transmitter	89
GPIO03/ PWM1/ RS232_RX	I/O w/5V-tolerant/ Output/ I/O w/ 5V-tolerant	General Purpose Input/Output; 4mA driving strength/ Pulse Width Modulation Output/ UART Receiver	90
GPIO04/ MSCL0/ PASS_SCL	I/O w/ 5V-tolerant/	General Purpose Input/Output; 4mA driving strength/ Master I2C Clock / I2C Bypass Clock	91

Pin Name	Pin Type	Function	Pin
GPIO05/ MSDA0/ PASS_SDA/ DP_HPD	I/O w/ 5V-tolerant/	General Purpose Input/Output; 4mA driving strength/ Master I2C Data / I2C Bypass Data/ HOTPLUG for DP Interface	92
GPIO06/ PWM4/ DP_SDM	I/O w/5V-tolerant/ Output/ Input	General Purpose Input/Output; 4mA driving strength / Pulse Width Modulation Output/ Cable Detection for DP	93
GPIO20/ PWM2	I/O w/5V-tolerant/ Output	General Purpose Input/Output; 8/16mA driving strength/ Pulse Width Modulation Output	204
GPIO21/ PWM3	I/O w/5V-tolerant/ Output	General Purpose Input/Output; 8/16mA driving strength/ Pulse Width Modulation Output	205
GPIO22/ PWM4/ SAR4	I/O w/5V-tolerant/ Output/ I/O w/ 5V-tolerant	General Purpose Input/Output; 4mA driving strength/ Pulse Width Modulation Output/ SAR ADC Input	206
GPIO23/ PWM5/ SAR5	I/O w/5V-tolerant/ Output/ Input	General Purpose Input/Output; 4mA driving strength/ Pulse Width Modulation Output/ SAR ADC Input	207
GPIO24/ CEC3/ PWM6	I/O w/5V-tolerant/ I/O / Output	General Purpose Input/Output; 4mA driving strength with 27Kohm pull high / HDMI Consumer Electrics Control(CEC) Bus IO with 27Kohm pull high/ Pulse Width Modulation Output	208
GPIO25/ CEC2/ PWM7	I/O w/5V-tolerant/ I/O / Output	General Purpose Input/Output; 4mA driving strength with 27Kohm pull high / HDMI Consumer Electrics Control(CEC) Bus IO with 27Kohm pull high/ Pulse Width Modulation Output	209
GPIO26/ CEC	I/O w/5V-tolerant/ I/O	General Purpose Input/Output; 4mA driving strength with 27Kohm pull high / HDMI Consumer Electrics Control(CEC) Bus IO with 27Kohm pull high	210
GPIO27/ IR	I/O w/ 5V-tolerant/ Input	General Purpose Input/Output; 4mA driving strength/ IR Input	211
GPIO40/ DDCA_CK/ RS232_RX	I/O w/ 5V-tolerant	General Purpose Input/Output; 4mA driving strength/ DDC Clock for Analog Input/ UART Receiver	70
GPIO41/ DDCA_DA/ RS232_TX	I/O w/ 5V-tolerant	General Purpose Input/Output; 4mA driving strength/ DDC Data for Analog Input/ UART Transmitter	71

Pin Name	Pin Type	Function	Pin
GPIO42/ PWM6	I/O w/5V-tolerant/ Output	General Purpose Input/Output; 4mA driving strength/ Pulse Width Modulation Output	72
GPIO43/ PWM7	I/O w/5V-tolerant/ Output	General Purpose Input/Output; 4mA driving strength/ Pulse Width Modulation Output	73
GPIO44/ PWM8	I/O w/5V-tolerant/ Output	General Purpose Input/Output; 4mA driving strength/ Pulse Width Modulation Output	74
GPIO45/ PWM9	I/O w/5V-tolerant/ Output	General Purpose Input/Output; 4mA driving strength/ Pulse Width Modulation Output	75
GPIO54/ PWM0/ EXTINT0	I/O w/5V-tolerant/ Output/ Input	General Purpose Input/Output; 4mA driving strength / Pulse Width Modulation Output/ External Interrupt Input	198
GPIO55/ PWM1/ EXTINT1	I/O w/5V-tolerant/ Output/ Input	General Purpose Input/Output; 4mA driving strength / Pulse Width Modulation Output/ External Interrupt Input	199
GPIO56/ PWM8/ EXTINT2	I/O w/5V-tolerant/ Output/ Input	General Purpose Input/Output; 4mA driving strength / Pulse Width Modulation Output/ External Interrupt Input	200
GPIO57/ PWM9/ EXTINT3	I/O w/5V-tolerant/ Output/ Input	General Purpose Input/Output; 4mA driving strength / Pulse Width Modulation Output/ External Interrupt Input	201
SAR0/ GPIO_SAR0	Input/ I/O w/5V-tolerant	SAR ADC Input/ General Purpose Input/Output; 4mA driving strength	212
SAR1/ GPIO_SAR1	Input/ I/O w/5V-tolerant	SAR ADC Input/ General Purpose Input/Output; 4mA driving strength	213
SAR2/ GPIO_SAR2	Input/ I/O w/5V-tolerant	SAR ADC Input/ General Purpose Input/Output; 4mA driving strength	214
SAR3/ GPIO_SAR3	Input/ I/O w/5V-tolerant	SAR ADC Input/ General Purpose Input/Output; 4mA driving strength	215

Misc. Interface

Pin Name	Pin Type	Function	Pin
AUXN	Input	Negative Display Port AUX channel	34
AUXP	Input	Positive Display Port AUX channel	35
GPIO_X10/ SAR10	I/O w/5V-tolerant / Input	General Purpose Input/Output; 4mA driving strength/ SAR ADC Input	1
GPIO_X11/ CABLE5V1	I/O w/5V-tolerant / Input	General Purpose Input/Output; 4mA driving strength/ Cable 5V for HPD Internal Pull High 1K	2
GPIO_X12/ HPD1	I/O w/5V-tolerant / Input	General Purpose Input/Output; 4mA driving strength / HOTPLUG for High-speed HDMI Interface Main Link0	8
GPIO_X13/ DDCD3_CK/ RS232_RX	I/O w/5V-tolerant	General Purpose Input/Output; 4mA driving strength/ DDC Clock for High-speed HDMI Interface Main Link0/ UART Receiver	3
GPIO_X14/ DDCD3_DA/ RS232_TX	I/O w/5V-tolerant	General Purpose Input/Output; 4mA driving strength/ DDC Data for High-speed HDMI Interface Main Link0/ UART Transmitter	4
GPIO_X30/ SAR8	I/O w/5V-tolerant/ Input	General Purpose Input/Output; 4mA driving strength/ SAR ADC Input	232
GPIO_X31/ CABLE5V3	I/O w/5V-tolerant/ Input	General Purpose Input/Output; 4mA driving strength/ Cable 5V for HPD Internal Pull High 1K	233
GPIO_X32/ HPD3	I/O w/5V-tolerant/ Input	General Purpose Input/Output; 4mA driving strength / HOTPLUG for DVI/HDMI Interface Main Link0	234
GPIO_X33/ RS232_RX/ DDCD0_CK	I/O w/5V-tolerant	General Purpose Input/Output; 4mA driving strength/ UART Receiver / DDC Clock and HDCP Slave Serial Port Clock for DVI/HDMI Interface Main Link0	235
GPIO_X34/ RS232_TX/ DDCD0_DA	I/O w/5V-tolerant	General Purpose Input/Output; 4mA driving strength/ UART Transmitter / DDC Data and HDCP Slave Serial Port Data for DVI/HDMI Interface Main Link0	236
GPIO_X40/ SAR7	I/O w/5V-tolerant/ Input	General Purpose Input/Output; 4mA driving strength/ SAR ADC Input	227
GPIO_X41/ CABLE5V4	I/O w/5V-tolerant/ Input	General Purpose Input/Output; 4mA driving strength/ Cable 5V for HPD Internal Pull High 1K	228
GPIO_X42/ HPD4	I/O w/5V-tolerant/ Input	General Purpose Input/Output; 4mA driving strength / HOTPLUG for DVI/HDMI Interface Main Link1	229
GPIO_X43/ RS232_RX/ DDCD1_CK	I/O w/5V-tolerant	General Purpose Input/Output; 4mA driving strength/ UART Receiver / DDC Clock and HDCP Slave Serial Port Clock for DVI/HDMI Interface Main Link1	230

Pin Name	Pin Type	Function	Pin
GPIO_X44/ RS232_TX/ DDCD1_DA	I/O w/5V-tolerant	General Purpose Input/Output; 4mA driving strength/ UART Transmitter / DDC Data and HDCP Slave Serial Port Data for DVI/HDMI Interface Main Link1	231
CID	Input	CID Detect	100
RESET	Input w/5V-tolerant	Chip Reset; High Reset	77
USB_DM	Input / Output	USB2.0 OTG Inverting Data Input/Output	104
USB_DP	Input / Output	USB2.0 OTG Non Inverting Data Input/Output	105
VBUS	Input	VBUS Detect	101
XIN	Analog Input	Crystal Oscillator Input	96
XOUT	Analog Output	Crystal Oscillator Output	95

Serial Flash Interface

Pin Name	Pin Type	Function	Pin
SCK	Output	SPI Flash Serial Clock	84
CSZ	Output	SPI Flash Chip Select	81
SDI	Output	SPI Flash Serial Data Input	83
SDO	Input w/ 5V-tolerant	SPI Flash Serial Data Output	82
(/WP)/ GPIO10	I/O w/ 5V-tolerant	SPI Flash Write Protect/ General Purpose Input/Output; 4mA driving strength	85
(/HOLD)/ GPIO11	I/O w/ 5V-tolerant	SPI Flash Hold/ General Purpose Input/Output; 4mA driving strength	86

Power Pins Interface

Pin Name	Pin Type	Function	Pin
AVDD_ADC	3.3V Power	Analog Power for ADC	43
AVDD_AUDIO	3.3V Power	Analog Power for Audio	53, 63
AVDD_LPLL	3.3V Power	Analog Power for LPLL	152
AVDD_MOD	3.3V Power	Analog Power for Panel Interface	125, 135, 170
AVDD_PLL	3.3V Power	Analog Power for PLL	97, 108, 219
AVDD_U33	3.3V Power	Analog Power	102
AVDDL_MOD	1.15V Power	Digital Power for Panel Interface	120, 138, 167
AVDDL_PREDRV	1.15V Power	Digital Power for Panel Interface	118, 136, 169
AVDD_HRX0	3.3V Power	Analog Power for High-speed HDMI	11
AVDD_DP	3.3V Power	Analog Power for DP	22

Pin Name	Pin Type	Function	Pin
AVDD_RX	3.3V Power	Analog Power for HDMI	248
AVDDL_HRX0	1.15V Power	Analog Power for High-speed HDMI	17, 18
AVDDL_DP	1.15V Power	Analog Power for DP	28
AVDDL_RX	1.15V Power	Analog Power for HDMI	238
VDD	1.15V Power	Digital Core Power	7, 39, 99, 111, 116, 151, 183, 216, 222, 237
VDDP	3.3V Power	Digital Input/Output Power	5, 80, 192, 203
VDD_NODIE	1.15V Power	LDO Output power (need add cap)	79, 193
DVDD_DDR_A	1.15V Power	DDR PAD Power	106
DVDD_DDR_RX_A	1.15V Power	DDR PAD Power	107
DVDD_DDR_B	1.15V Power	DDR PAD Power	217
DVDD_DDR_RX_B	1.15V Power	DDR PAD Power	218
VDDIO_A	1.8V Power	DDR PAD Power	109, 110, 112
VDDIO_B	1.8V Power	DDR PAD Power	220, 221, 223
VDD_DRAM_A	1.8V Power	DDR PAD Power	113-115
VDD_DRAM_B	1.8V Power	DDR PAD Power	224-226
GND	Ground	Ground	6, 14, 21, 25, 31, 40, 41, 42, 60, 76, 78, 94, 98, 103, 117, 119, 126, 137, 153, 166, 168, 202, 247

No Connection

Pin Name	Pin Type	Function	Pin
NC	-	No connect. Leave this pin floating.	36-38

ELECTRICAL SPECIFICATIONS

Analog Interface Characteristics

Parameter	Min	Typ	Max	Unit
VIDEO ADC Resolution		10		Bits
DC ACCURACY				
Differential Nonlinearity	-1		1.5	LSB
Integral Nonlinearity	-3		3	LSB
VIDEO ANALOG INPUT				
Input Voltage Range	0.8		1.1	V p-p
Input Full-Scale Matching		1.5		%FS
Brightness Level Adjustment		62		%FS
Sync-On-Green Amplitude		0.3		V p-p
SWITCHING PERFORMANCE				
Maximum Conversion Rate	202.5			MSPS
Minimum Conversion Rate			12	MSPS
HSYNC Input Frequency	15		200	kHz
VSYNC Input Frequency	10		200	Hz
PLL Clock Rate	12		202.5	MHz
PLL Jitter		500		ps p-p
Sampling Phase Tempco		15		ps/°C
DIGITAL INPUTS				
Input Voltage, High (V_{IH})	2.0			V
Input Voltage, Low (V_{IL})			0.8	V
Input Current, High (I_{IH})			-1.0	uA
Input Current, Low (I_{IL})			1.0	uA
Input Capacitance		5		pF
DIGITAL OUTPUTS				
Output Voltage, High (V_{OH})	VDDP-0.4			V
Output Voltage, Low (V_{OL})			0.4	V
AUDIO				
ADC Input		2.8		V p-p
DAC Output		2.8		V p-p
SAR ADC Input	0		3.3	V
GPIO Interface				
Input Voltage, High (VIH)			2.0	V
Input Voltage, Low (VIL)	0.8			V

Specifications subject to change without notice.
Note: Input full scale is 1.0V, but input range is 0 ~ 3.3V.
VDDP is 3.3V supply voltages

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
3.3V Supply Voltages	V_{VDD_33}	3.14		3.46	V
1.8V Supply Voltages	V_{VDD_18}	1.71		1.89	V
1.15V Supply Voltages	V_{VDD_115}	1.09	1.15	1.21	V
Ambient Operating Temperature	T_A	0		70	°C
Junction Temperature	T_J			125	°C

Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
3.3V Supply Voltages	V_{VDD_33}		3.63	V
1.8V Supply Voltages	V_{VDD_18}		1.98	V
1.15V Supply Voltages	V_{VDD_115}		1.26	V
Input Voltage (5V tolerant inputs)	$V_{IN5Vtol}$		5.3	V
Input Voltage (non 5V tolerant inputs)	V_{IN}		V_{VDD_33}	V
Storage Temperature	T_{STG}	-40	150	°C

Note: Stresses above those listed in Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and does not imply functional operation of the device. Exposure to absolute maximum ratings for extended periods may affect device reliability.