LONTIUM SEMICONDUCTOR CORPORATION

ClearEdge™ Technology

LT8711HE

Type-C/DP1.2 to HDMI2.0 Converter

Datasheet

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1. Features

- **USB Type-C**
  - Compliant with VESA DisplayPort Alt Mode on USB Type-C standard V1.0
  - Compliant with USB Power Delivery specification R2.0, V1.0
  - Compliant with USB Type-C Cable and Connector specification R1.2
  - Compliant with HDMI 1.4b Alt Mode on USB Type-C specification V1.0
  - Compliant with DP Alt Mode 1.0, PD 2.0, Type-C 1.2, HDMI1.4b Alt Mode 1.0
  - Built-in dual CC controllers for charger and normal communication
  - 3 data roles supported: DFP, UFP and DRP
  - 2 power roles supported: source and sink
- **DP1.2 Receiver**
  - Compliant with VESA DP1.2 and Embedded DisplayPort (eDP) v1.4
  - No HDCP decryption
  - 1/2/4 configurable data lanes
  - 1.62/2.7/5.4Gbps per data lane
  - Support SSC
  - 1Mbps AUX channel
  - Receiver PHY is HDMI signal compatible
  - Adaptive or programmable receiver equalization
  - Support lane swap(arbitrarily) and polarity inversion(independent)
  - Support 4k@60Hz
  - Support eDP Authentication: Alternative Scramble Seed Reset and Alternative Framing
  - Fast and full Link Training for Embedded DisplayPort system
- **HDMI2.0 Transmitter**
  - Compliant with HDMI2.0, HDMI1.4 and DVI1.0
  - Data rate up to 6Gbps
  - Support 4k@60Hz
  - Support TMDS scrambling for EMI/RFI reduction
  - Support SCDC
  - Support channel swap(arbitrarily) and polarity inversion(independent)
  - Programmable transmitter swing and pre-emphasis
  - Downstream receiver sensing
  - 5V tolerance DDC/HPD I/Os
- **Miscellaneous**
  - DP receiver to HDMI transmitter bypass to support HDMI Alt Mode
  - Support Swift Charge
  - USB billboard module and USB2.0 switch integrated
  - Internal or external oscillator
  - Integrated microprocessor
  - Embedded SPI flash for firmware
  - GPIOs for VBUS/VCONN/AUX and other system controls
  - Integrated 100/400kHz I2C slave
  - Firmware update through SPI, I2C, AUX or USB interface
  - Low power consumption
  - Power supply: 3.3V for I/O and 1.2V for core
  - Embedded 5V to 3.3V LDO
  - ESD 4kV HBM
  - Temperature range: -40°C ~ +85°C
  - Package：7.5mmx7.5mm QFN64

2. Description

The LT8711HE is a high performance Type-C/DP1.2 to HDMI2.0 converter, designed to connect a USB Type-C source or a DP1.2 source to an HDMI2.0 sink.

The LT8711HE integrates a DP1.2 compliant receiver, and an HDMI2.0 compliant transmitter. Also, two CC controllers are included for CC communication to implement DP Alt Mode and power delivery function, one

for upstream Type-C port and another for downstream port. The device is capable of automatic operation which is enabled by an integrated microprocessor that uses a embedded SPI flash for firmware storage. System control is also available through the use of a dedicated configuration I2C slave interface.

LT8711HE also support EDID buffer, DP/eDP input detection and determine to enter into power saving mode automatically. When the receiver of LT8711HE locks the input signal, the MCU can read the recovered timing parameters by the MSA registers to match the ASSR. The DPCD registers are accessible via system I2C when debugging the full link training. Once the fast

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link training used, system time will save at least 400ms.

3. Applications

- Docking Station
- Dongle

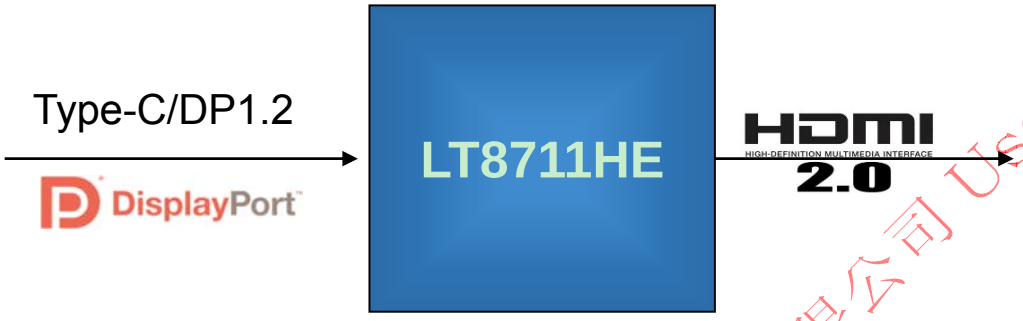

Figure 3.1 Application Diagram

4. Ordering Information

Table 4.1 Ordering Information

Part Number	Operating Temperature Range	Package	Packing Method
LT8711HE	-40℃ to+85℃	QFN64 (7.5*7.5)	Tray

5. Revision History

Version	Owner	Content	Date
R1.0	Terry	Initial datasheet creation	08/18/2017
R1.1	Terry	Update pin assignment	11/23/2017
R1.2	Terry	Update electrical characteristics information	12/12/2017
	N W	Update package information	11/15/2018
R1.3	Terry	Update about power consumption and reset sequence information	05/25/2019
R1.4	PP J	Update Figure 6.1.1	07/26/2019

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6. Pinning Information

6.1 Pin Configuration

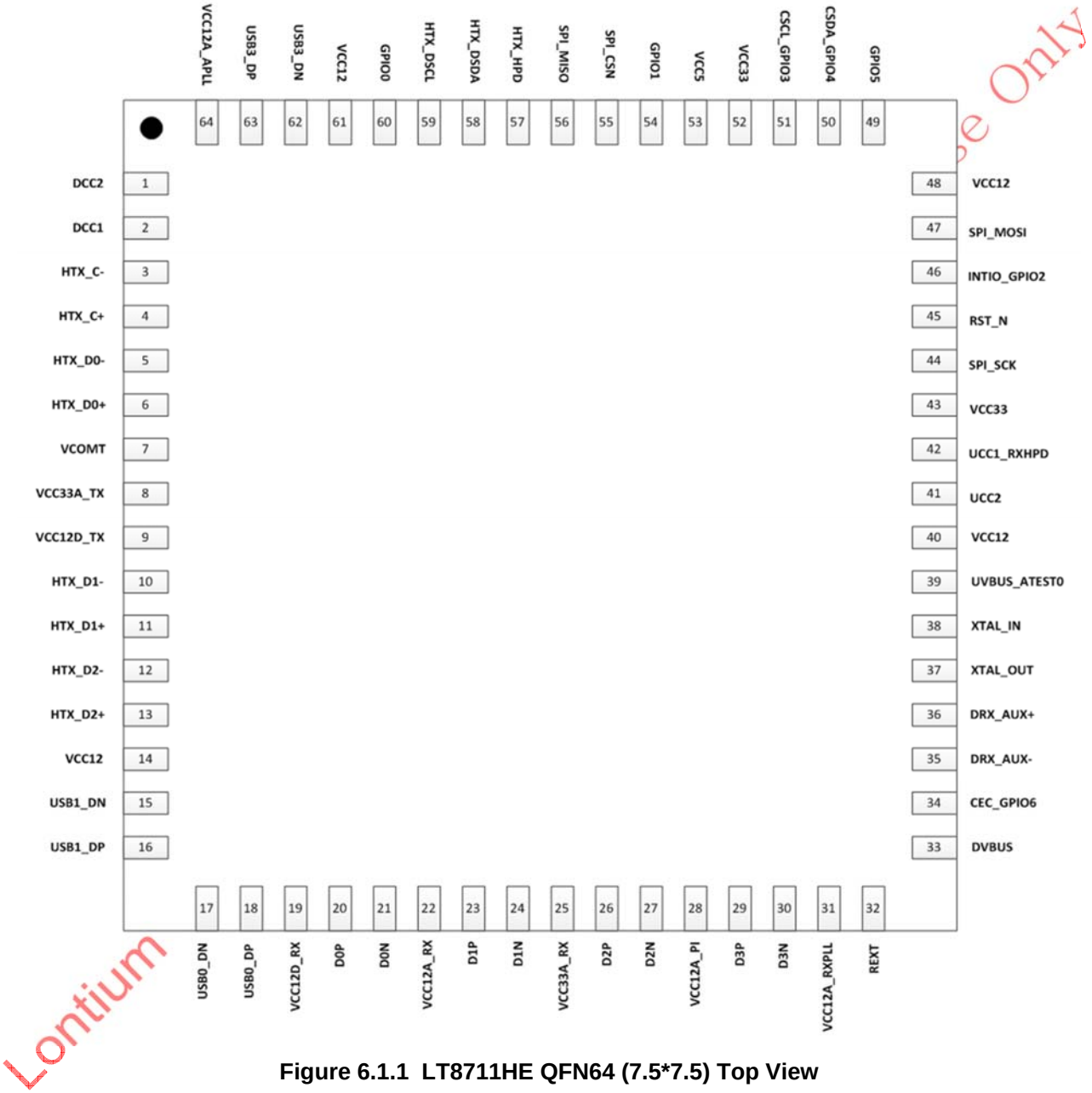

Figure 6.1.1 LT8711HE QFN64 (7.5*7.5) Top View

To minimize the power supply noise floor, at least one 0.1μF and one 0.01μF decoupling capacitors recommended to be installed near all the LT8711HE power pins. To avoid large current loops and trace inductance, the trace length between decoupling capacitor and device power inputs pins must be minimized.

6.2 Pin Description

Table 6.2.1 Pin Description

Pin#	Pin Name	I/O Type	I/O Dir	Description
65	VSS	G	I/O	Ground(EPAD)
53	VCC5	P	I/O	5V Power for LDO
8	VCC33A_TX	P	I/O	3.3V Power for HDMI TX
25	VCC33A_RX	P	I/O	3.3V Power for DP RX
43,52	VCC33	P	I/O	3.3V IO Power
14,40,48,61	VCC12	P	I/O	1.2V Core Power
64	VCC12A_APLL	P	I/O	1.2V Power for Audio PLL
9	VCC12D_TX	P	I/O	1.2V Power for HDMI TX
19	VCC12D_RX	P	I/O	1.2V Power for DP RX
22	VCC12A_RX	P	I/O	1.2V Power for DP RX
28	VCC12A_PI	P	I/O	1.2V Power for DP RXPI
31	VCC12A_RXPLL	P	I/O	1.2V Power for DP RXPLL
3	HTX_C-	Analog	O	HDMI Clock Channel Negative Output Maximum clock rate is 340MHz.
4	HTX_C+	Analog	O	HDMI Clock Channel Positive Output Maximum clock rate is 340MHz.
5	HTX_D0-	Analog	O	HDMI Data Channel 0 Negative Output Maximum data rate is 6Gbps.
6	HTX_D0+	Analog	O	HDMI Data Channel 0 Positive Output Maximum data rate is 6Gbps.
10	HTX_D1-	Analog	O	HDMI Data Channel 1 Negative Output Maximum data rate is 6Gbps.
11	HTX_D1+	Analog	O	HDMI Data Channel 1 Positive Output Maximum data rate is 6Gbps.
12	HTX_D2-	Analog	O	HDMI Data Channel 2 Negative Output Maximum data rate is 6Gbps.
13	HTX_D2+	Analog	O	HDMI Data Channel 2 Positive Output Maximum data rate is 6Gbps.
7	VCOMT	Analog	O	HDMI TX Ground Detect Input for AC Couple Mode
15	USB1_DN	Analog	I/O	USB 2.0 Output Pin
16	USB1_DP	Analog	I/O	USB 2.0 Output Pin
17	USB0_DN	Analog	I/O	D- Input of USB Type C Interface
18	USB0_DP	Analog	I/O	D+ Input of USB Type C Interface
29	D3P	Analog	I	RX Data Channel Lane-3 Positive Input Maximum data rate is 5.4Gbps.
30	D3N	Analog	I	RX Data Channel Lane-3 Negative Input Maximum data rate is 5.4Gbps.
26	D2P	Analog	I	RX Data Channel Lane-2 Positive Input Maximum data rate is 5.4Gbps.
27	D2N	Analog	I	RX Data Channel Lane-2 Negative Input Maximum data rate is 5.4Gbps.
23	D1P	Analog	I	RX Data Channel Lane-1 Positive Input Maximum data rate is 5.4Gbps.
24	D1N	Analog	I	RX Data Channel Lane-1 Negative Input Maximum data rate is 5.4Gbps.

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Pin#	Pin Name	I/O Type	I/O Dir	Description
20	D0P	Analog	I	RX Data Channel Lane-0 Positive Input Maximum data rate is 5.4Gbps.
21	D0N	Analog	I	RX Data Channel Lane-0 Negative Input Maximum data rate is 5.4Gbps.
36	DRX_AUX+	Analog	I/O	AUX Positive Input
35	DRX_AUX-	Analog	I/P	AUX Negative Input
38	XTAL_IN	Analog	I/O	Crystal Oscillator Input
37	XTAL_OUT	Analog	I/O	Crystal Oscillator Output
32	REXT	Analog	O	External 7.68Kohm Resistor For BG
33	DVBUS	Analog	I/O	One Tenth of VBUS Connected with Sink
34	CEC_GPIO6	LVTTL, OD	I/O	HDMI CEC Signal or Used as GPIO
39	UVBUS_ATEST0	Analog	I/O	One Tenth of VBUS Connected with Source or GPO for TEST
42	UCC1_RXHPD	Analog	I/O	Type-C Configuration Channel, CC1 Connected with Source, HPD Signal Output for DP Mode
41	UCC2	Analog	I/O	Type-C Configuration Channel, CC2 Connected with Source
44	SPI_SCK	LVTTL	O	Clock for SPI Interface
45	RST_N	Schmitt	I	External Reset Signal, Low is Reset.
46	INTIO_GPIO2	LVTTL	I/O	GPIO
47	SPI_MOSI	LVTTL	O	MOSI for SPI Interface
49	GPIO5	LVTTL	I/O	GPIO
50	CSDA_GPIO4	Schmitt, OD	I/O	Slave I2C SDA Signal For Program Register
51	CSCL_GPIO3	Schmitt, OD	I	Slave I2C SCL Signal For Program Register
54	GPIO1	LVTTL	I/O	GPIO
55	SPI_CSN	LVTTL	O	Chip Select Signal for SPI Interface
56	SPI_MISO	Schmitt	I	MISO for SPI Interface
57	HTX_HPD	Schmitt	I	HPD Signal Of SINK
58	HTX_DSDA	Schmitt, OD	I/O	SINK DDC/SCDC Channel DSDA Signal
59	HTX_DSCL	Schmitt, OD	O	SINK DDC/SCDC Channel DSCL Signal
60	GPIO0	LVTTL	I/O	GPIO
62	USB2_DN	Analog	I/O	USB Negative Terminal for Swift Charge
63	USB2_DP	Analog	I/O	USB Positive Terminal for Swift Charge
2	DCC1	Analog	I/O	Type-C Configuration Channel, CC1 Connected with Sink
1	DCC2	Analog	I/O	Type-C Configuration Channel, CC2 Connected with Sink

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7. Function Description

7.1 Function Block Diagram

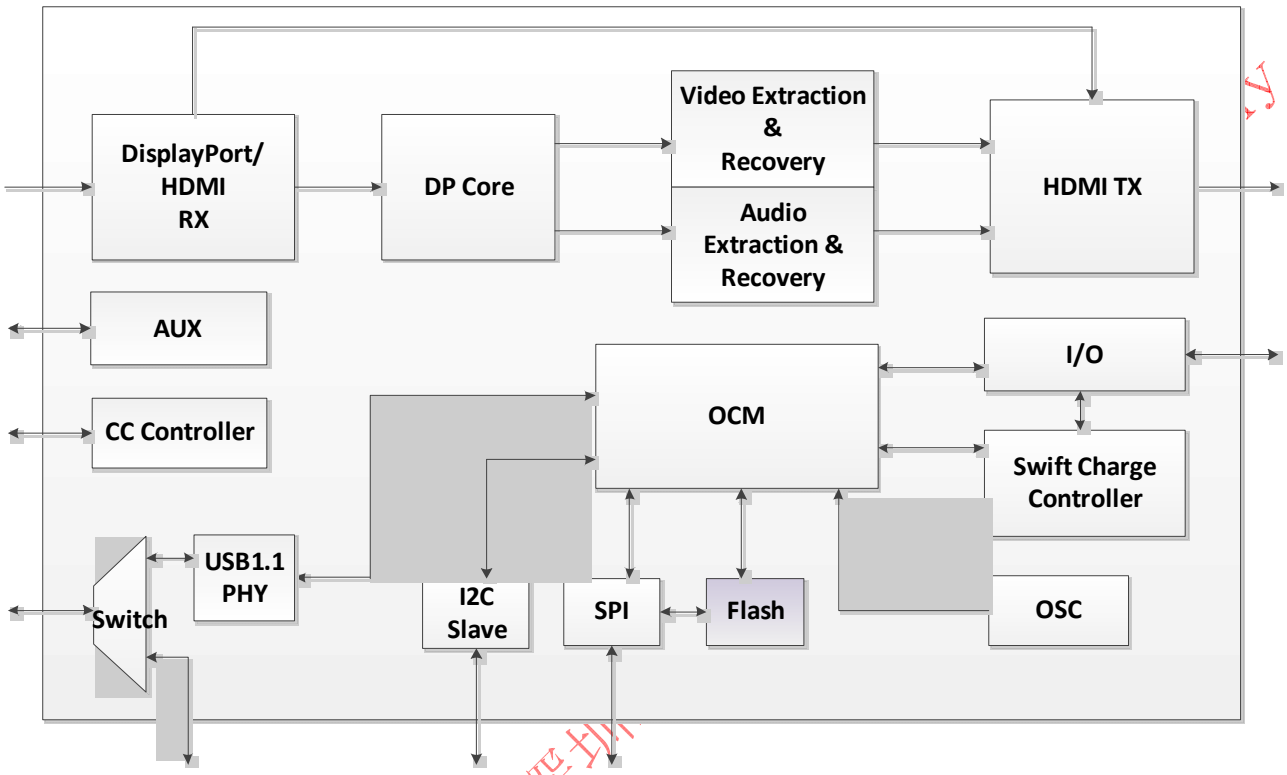

Figure 7.1.1 Function Block Diagram

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8. Electrical Characteristics

8.1 Absolute Maximum Conditions

Table 8.1.1 Absolute Maximum Conditions

Symbol	Description	Min	Typ	Max	Unit
VCC5	5V Power Supply Voltage	-0.3		5.5	V
VCC33A_TX,VCC33A_RX, VCC33	3.3V Power Supply Voltage	-0.3		3.63	V
VCC12, VCC12A_APLL, VCC12D_TX, VCC12D_RX, VCC12A_RX, VCC12A_PI, VCC12A_RXPLL	1.2V Power Supply Voltage	-0.3		1.32	V
V_I	CMOS Terminal Input Voltage Range	-0.3		3.63	V
V_O	CMOS Terminal Output Voltage Range	-0.3		3.63	V
T_S	Storage Temperature	-55		125	℃
ESD	HBM Elastrostatic Discharge Level		4000		V

Notes:
1.Permanent device damage may occur if absolute maximum conditions are exceeded.
2.Function operation should be restricted to the conditions described under Normal Operating Conditions.

8.2 Normal Operating Conditions

Table 8.2.1 Normal Operating Conditions

Symbol	Description	Min	Typ	Max	Unit
VCC5	5V Power Supply Voltage	4.5	5	5.5	V
VCC33A_TX,VCC33A_RX, VCC33	3.3V Power Supply Voltage	2.97	3.3	3.63	V
VCC12, VCC12A_APLL, VCC12D_TX, VCC12D_RX, VCC12A_RX, VCC12A_PI, VCC12A_RXPLL	1.2V Power Supply Voltage	1.08	1.2	1.32	V
VCC_N	Power Supply Voltage Noise			50	mV
T_A	Operating Free-air Temperature	-40	27	85	℃

8.3 DC Characteristics

Table 8.3.1 DC Characteristics

DP RX DC Specifications

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Symbol	Description	Min	Typ	Max	Unit
V_{idiff}	Differential input peak-peak voltage level	90			mV
R_{term}	Single-ended termination resistance	45	50	55	Ω
HDMI Receiver DC Specifications					
Symbol	**Description**	**Min**	**Typ**	**Max**	**Unit**
V_{idiff}	Input differential voltage level	150		1200	mV
V_{icm}	Input common mode voltage	AVCC-700		AVCC-37.5	mV
AVCC	Termination supply voltage	3.3±5%			V
RT	Termination resistance	50±10%			Ω
HDMI Transmitter DC Specifications					
Symbol	**Description**	**Min**	**Typ**	**Max**	**Unit**
VOFF	Single-ended standby (off) output voltage	AVCC-10		AVCC+10	mV
VH	Single-ended output high level voltage	AVCC-400		AVCC+10	mV
VL	Single-ended output low level voltage	AVCC-1000		AVCC-400	mV
VSWING	Single-ended output data swing	400		600	mV
RTERM	AC couple single-ended impedance	40		60	Ω

8.4 AC Characteristics

Table 8.4.1 AC Characteristics

DP RX AC Specifications					
Symbol	**Description**	**Min**	**Typ**	**Max**	**Unit**
$T_{rx\_eye\_conn\_RBR}$	Minimum Receiver EYEWidth at RX-sideconnector pins for RBR	0.25			UI
$T_{rx\_eye\_conn\_HBR2}$	Minimum Receiver EYEWidth at RX-sideconnector pins for HBR2	0.38			UI
$T_{intra\_skew\_HRB2}$	Intra-pair skew at sink connector for HBR2			50	ps
$T_{intra\_skew\_HRB}$	Intra-pair skew at sink connector for HBR			60	ps
$T_{intra\_skew\_RBR}$	Intra-pair skew at sink connector for RBR			260	ps
TMDS RX AC Specifications					
Symbol	**Description**	**Min**	**Typ**	**Max**	**Unit**
V_s	Minimum differential sensitivity(peak to peak) after the reference cable equalizer	150			mV
T_{intra_skew}	Intra-pair skew at sink connector			0.15T+112	ps
T_{inter_skew}	Inter-pair skew at sink connector			0.2Tcharactor+1.78	ns
T_{jitter}	TMDS clock jitter			0.3Tbit	ps
TMDS TX AC Specifications@TP1					
Symbol	Parameter	MIN	TYP	MAX	Unit
T_{intra_skew}	Intra-pair skew			0.15	ps

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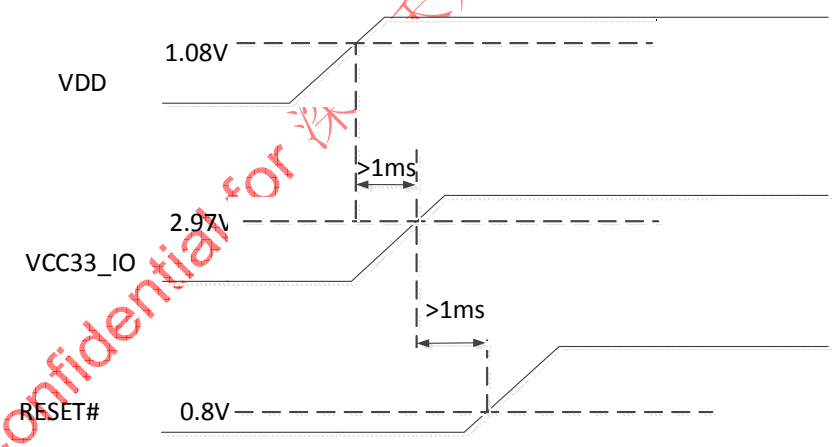
				Tbit	
T_{inter_skew}	Inter-pair skew			0.2 Tcharac tor	ns
V_{d_high}	Maximum differential voltage			780	mV
V_{d_low}	Minimum differential voltage	-780			mV
T_{jitter}	Maximum TMDS clock jitter			0.3Tbit	ps

8.5 Power Consumption

Table 8.5.1 Power Consumption

Condition		Supply Current(3.3V)	Supply Current(1.2V)	Unit
4k@60Hz	4lane@5.4G	41	575	mA
4k@30Hz	2lane@5.4G	35	466	mA
	4lane@2.7G	30	390	mA
1080p@60Hz	1lane@5.4G	35	426	mA
	2lane@2.7G	30	334	mA
	4lane@1.62G	29	290	mA

8.6 Power-up and Reset Sequence



Note:

（1）3.3V power should be set up at least 1ms later than 1.2V power, the internal reset signal should be released after 3.3V power is ready.

（2）External RESET# signal should be set up at least 1ms later than 3.3V.

Figure 8.6.1 Power-up and Reset Sequence

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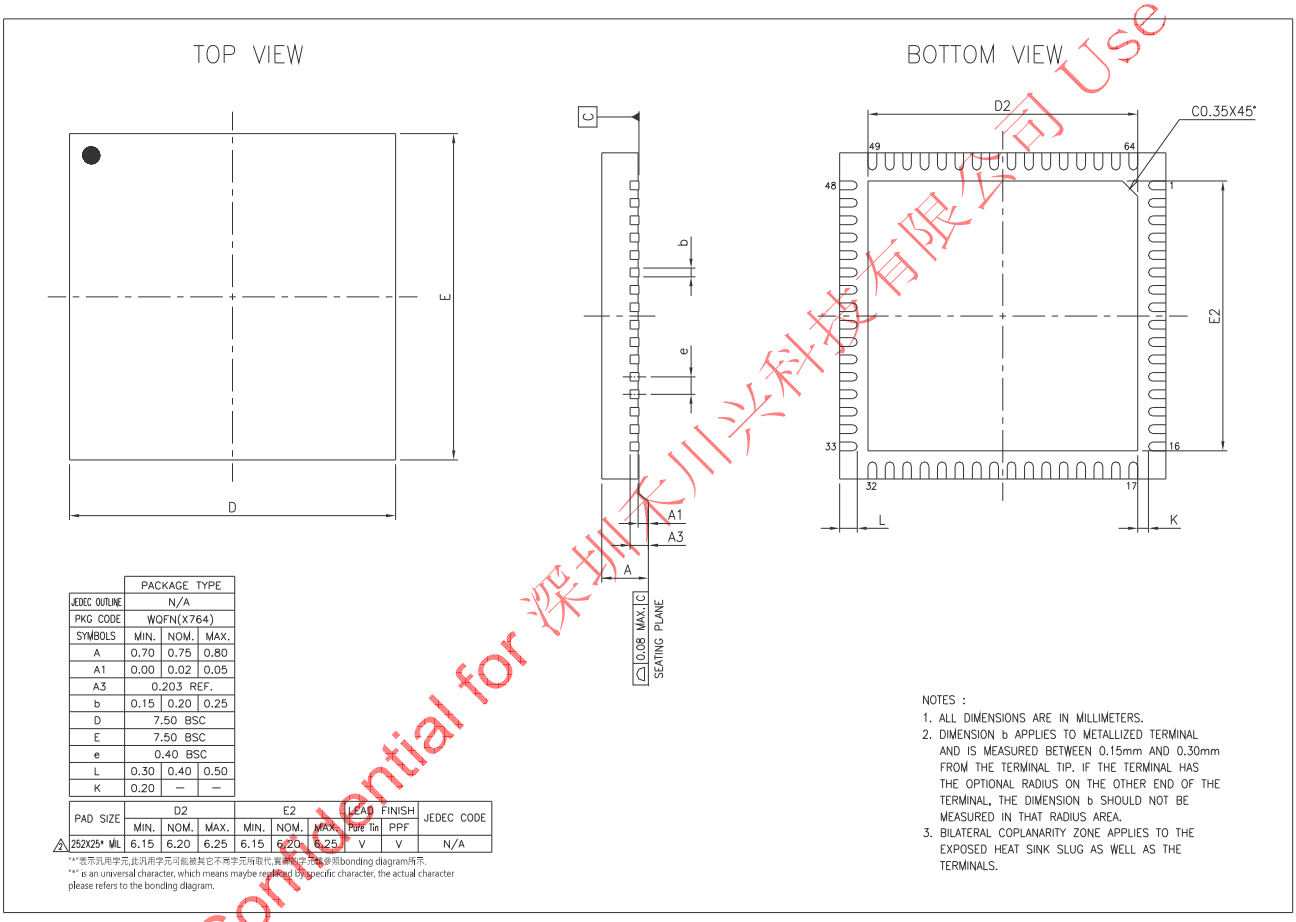
9. Package Information

The LT8711HE is packaged in a 64-lead QFN package with ePad.

The ePad needs to be soldered to the PCB. The information in the following paragraphs is provided for applications which solder the ePad to the PCB.

The ePad must not be electrically connected to any other voltage level except ground (GND). A clearance of at least 0.25mm should be designed on the PCB between the edge of the ePad and the inner edges of the lead pads to avoid any electrical shorts.



	PACKAGE TYPE		
JEDEC OUTLINE	N/A		
PKG CODE	WQFN(X764)		
SYMBOLS	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3	0.203 REF.		
b	0.15	0.20	0.25
D	7.50 BSC		
E	7.50 BSC		
e	0.40 BSC		
L	0.30	0.40	0.50
K	0.20	–	–

PAD SIZE	D2			E2			LEAD FINISH		JEDEC CODE
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	Pure Tin	PPF	
⚠2 252X25* MIL	6.15	6.20	6.25	6.15	6.20	6.25	V	V	N/A

*A*表示汎用字元,此汎用字元可能被其它不同字元所取代,實際使用字元請參照bonding diagram所示.
A is an universal character, which means maybe replaced by specific character, the actual character please refers to the bonding diagram.

NOTES :
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15mm AND 0.30mm FROM THE TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION b SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
3. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.

Figure 9.1 Package Dimensions

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