VIA Labs, Inc.

Data Sheet

VL815
USB 3.1 Gen1 Hub Controller

July 1st , 2019

Revision 1.00

Revision History

Rev	Date	Note	Initial
1.00	07/01/2019	Initial release	EC

Contents

List of Figures

Product Features

VL815
USB 3.1 Gen1 4-Port Hub Controller

- **USB 3.1 Compliant**
  - Compliant to Universal Serial Bus 3.1 Specification
  - Meets all USB 3.1 ECN through Dec 2018
  - Compliant to Universal Serial Bus 2.0 Specification
  - USB 2.0 Hub Supports MTT
  - Supports Simultaneous Operation of Any Combination of SuperSpeed, High-Speed, Full-Speed, and Low-Speed Devices
  - Supports USB Power Saving Features such as Link Power Management, Ux States, Selective Suspend, and Function Suspend
  - In-house USB PHY employs advanced CMOS process for low power consumption

- **Full Sideband Signal Support**
  - Supports Ganged Mode Operation for All Ports
  - Management Interface by strapping pin for Specialized Applications

- **Comprehensive USB Battery Charging Support**
  - Supports USB Battery Charging Specification v1.2 (SDP, CDP)
  - Supports Stand-Alone Charging when System is Suspend, Shut Down, or Disconnected
  - Supporting Gang mode over-current detection for all downstream ports
  - Through Strapping to enable/disable CDP without FW (SPI flash) setting.

- **Power and Package**
  - Requires 3.3V and 1.1V Inputs
  - 25MHz Xtal
  - Integrated Voltage Regulators Generate All Required Voltages from 5V Input
    5V to 1.1V Switching DC-DC Regulator
    5V to 3.3V LDO Regulator
  - QFN 76L green package (9x9x0.85 mm)

VL815 System Overview

VIA Lab's VL815 is a modern USB 3.1 Gen1 Hub Controller, featuring an optimized cost-structure and full compliance with USB 3.1 Gen1 specification including ECNs and Compliance Testing Updates through Dec 2018. VL815 is offered in 4-port configurations, and features integrated voltage regulators, new lower-power design, and comprehensive USB Charging support. VL815 supports any combination of SuperSpeed (5Gbps), High Speed (480Mbps), Full Speed (12Mbps), and Low Speed (1.5Mbps) devices, and the integrated USB 2.0 hub's Multiple Transaction Translators feature provides increased performance when multiple Full Speed devices are simultaneously used. The integrated 5V DC-DC switching regulator enables VL815 to be powered directly from 5V USB VBus, reducing BOM cost while offering high power efficiency.

VL815-based hub devices work under Windows, Mac OS X, and various Linux kernels without additional drivers. VL815-based hub devices are also compatible with non-x86 devices and platforms that support USB hub functions such as smart phones, tablets, and set-top boxes. It is well suited for all USB hub applications such as standalone USB hubs, Notebook/Ultrabook docking stations/port-replicators, desktop PC front panel, motherboard on-board hub, and USB hub compound devices.

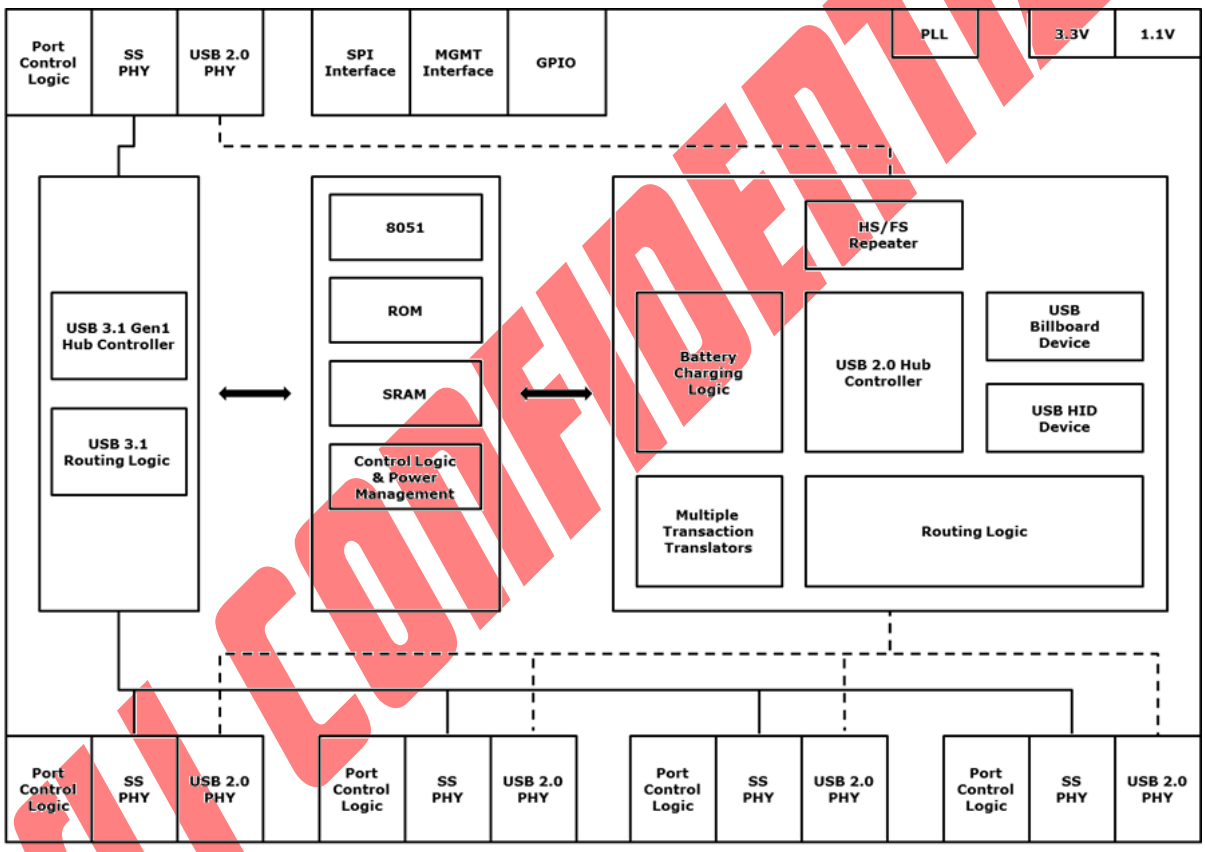


Figure 1 – VL815-Q7 Block Diagram

USB Battery Charging Behavior

Concepts of Rapid Charging over USB:

- **Rapid Charging over USB enables charging of devices at rates in excess of baseline USB standards.**

  The current limit of USB 2.0 is 500mA for configured devices, and the current limit of USB 3.0 is 900mA for configured devices. Depending on the device, Rapid Charging implementations typically feature current limits between 500mA to 1500mA.

- **It is the Host/Hub's responsibility to advertise Rapid Charging capabilities, and it is the Device's responsibility to recognize and determine those capabilities.**

  Rapid Charging over USB enables charging at rates in excess of baseline USB specifications, so in order to prevent a situation where a device sinks more current than what a port is rated for, different manufacturers employ various charging schemes in an attempt to ensure safe and reliable operation with their respective device and charger. It goes without saying that Rapid Charging will only occur when both Host/Hub and Device supports it.

- **The rate at which a device charges is dependent upon the device.**

  This means that the device must determine the host/hub port's capabilities to determine which charging mode to use. Also, the rate at which a device charges can vary depending on the status of the device. For example, some devices only charge at their maximum rate when the battery is nearly depleted. When the battery is nearly full, they may switch to a trickle-charge mode. The Host/Hub rapid-charging port has no control over this behavior.

Supported USB Charging Modes

SDP – Standard Downstream Port
This is a typical USB 2.0 or USB 3.0 port and does not explicitly support Rapid USB Charging. SDP is constrained to the current limits as defined in the USB 2.0 or USB 3.0 spec which are 500mA and 900mA respectively. While the actual current limit is enforced by the polyfuse or power-switch providing current-limiting functionality for the downstream port, most USB devices will not draw more than 500mA or 900mA under USB 2.0 or USB 3.0 modes.

CDP – Charging Downstream Port
CDP is defined in the USB Battery Charging Specification 1.2 and enables devices that are able to correctly recognize CDP to simultaneously function as a USB device while drawing up to 1.5A for Rapid Charging when connected to the downstream port of a USB Host or Hub that advertises CDP capability.

Pinout (VL815-Q7)

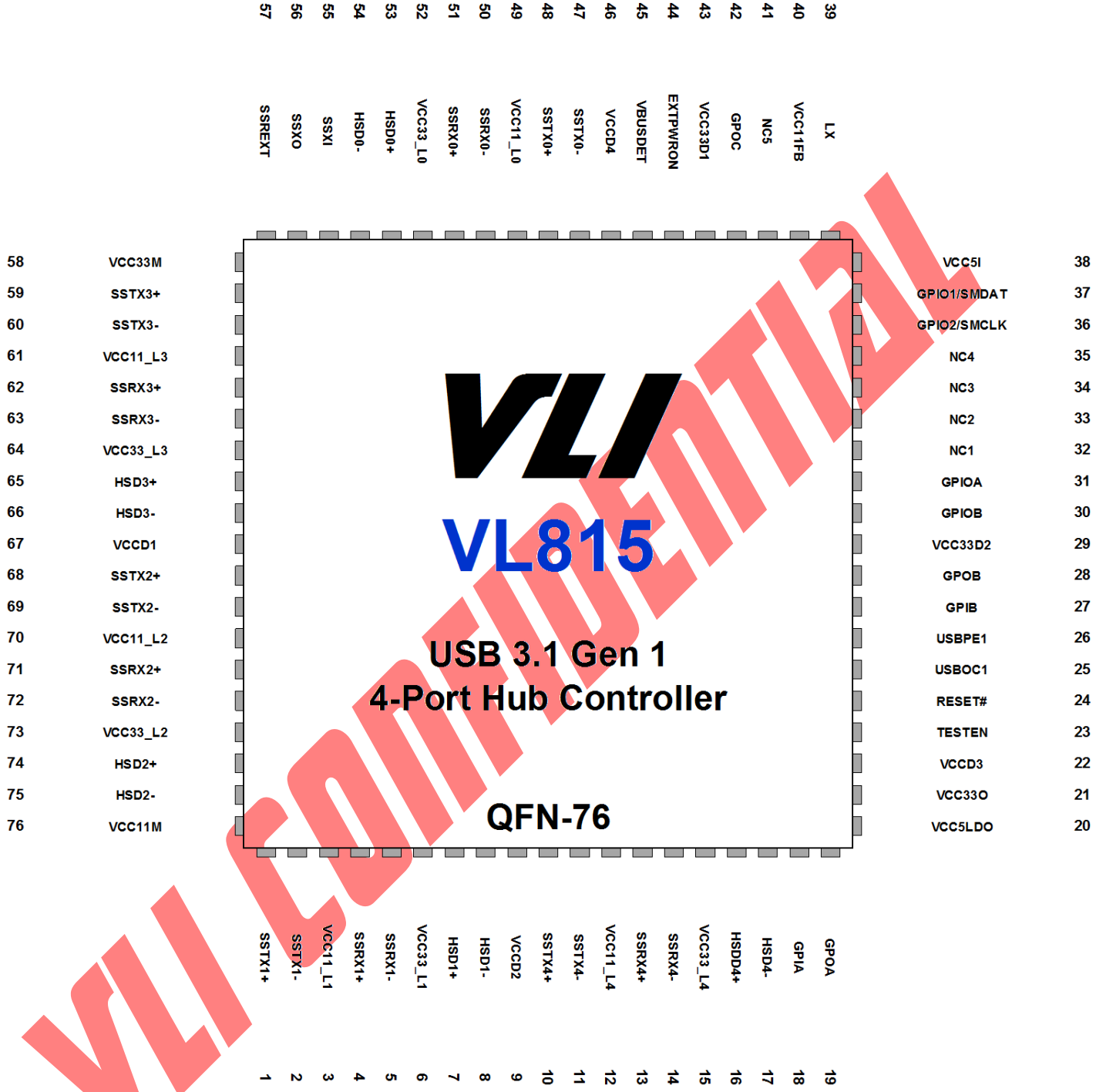


Figure 2 – VL815-Q7 Pin Diagram

Pin List (VL815-Q7)

Table 1 – VL815-Q7 Pin List

Pin	Pin Name	Pin	Pin Name
1	SSTX1+	39	LX
2	SSTX1-	40	VCC11FB
3	VCC11_L1	41	NC5
4	SSRX1+	42	GPOC
5	SSRX1-	43	VCC33D1
6	VCC33_L1	44	EXTPWRON
7	HSD1+	45	VBUSDET
8	HSD1-	46	VCCD4
9	VCCD2	47	SSTX0-
10	SSTX4+	48	SSTX0+
11	SSTX4-	49	VCC11_L0
12	VCC11_L4	50	SSRX0-
13	SSRX4+	51	SSRX0+
14	SSRX4-	52	VCC33_L0
15	VCC33_L4	53	HSD0+
16	HSD4+	54	HSD0-
17	HSD4-	55	SSXI
18	GPIA	56	SSXO
19	GPOA	57	SSREXT
20	VCCLDO5	58	VCC33M
21	VCC33O	59	SSTX3+
22	VCCD3	60	SSTX3-
23	TESTEN	61	VCC11_L3
24	RESET#	62	SSRX3+
25	USBOC1	63	SSRX3-
26	USBPE1	64	VCC33_L3
27	GPIB	65	HSD3+
28	GPOB	66	HSD3-
29	VCC33D2	67	VCCD1
30	GPIOB	68	SSTX2+
31	GPIOA	69	SSTX2-
32	NC1	70	VCC11_L2
33	NC2	71	SSRX2+
34	NC3	72	SSRX2-
35	NC4	73	VCC33_L2
36	GPIO2/SMCLK	74	HSD2+
37	GPIO1/SMDAT	75	HSD2-
38	VCC5I	76	VCC11M

Pin Descriptions (VL815-Q7)

Signal Type Definition

Name	Type	Signal Description
Input	I	A Logic Input Only Signal
Output	O	A Logic Output Only Signal
Input/Output	I/O	A Logic Bi-Directional Signal
Power	PWR	A Power Pin
Ground	GND	A Ground Pin
NC	-	No Connection Pin

USB 3.1 Interface

Pin Name	Pin #	I/O	Signal Description
SSTX0+	48	O	USB 3.1 UFP Differential TX+
SSTX0-	47	O	USB 3.1 UFP Differential TX–
SSRX0+	51	I	USB 3.1 UFP Differential RX+
SSRX0-	50	I	USB 3.1 UFP Differential RX–
SSTX1+	1	O	USB 3.1 DFP1 Differential TX+
SSTX1-	2	O	USB 3.1 DFP1 Differential TX–
SSRX1+	4	I	USB 3.1 DFP1 Differential RX+
SSRX1-	5	I	USB 3.1 DFP1 Differential RX–
SSTX2+	68	O	USB 3.1 DFP2 Differential TX+
SSTX2-	69	O	USB 3.1 DFP2 Differential TX–
SSRX2+	71	I	USB 3.1 DFP2 Differential RX+
SSRX2-	72	I	USB 3.1 DFP2 Differential RX–
SSTX3+	59	O	USB 3.1 DFP3 Differential TX+
SSTX3-	60	O	USB 3.1 DFP3 Differential TX–
SSRX3+	62	I	USB 3.1 DFP3 Differential RX+
SSRX3-	63	I	USB 3.1 DFP3 Differential RX–
SSTX4+	10	O	USB 3.1 DFP4 Differential TX+
SSTX4-	11	O	USB 3.1 DFP4 Differential TX–
SSRX4+	13	I	USB 3.1 DFP4 Differential RX+
SSRX4-	14	I	USB 3.1 DFP4 Differential RX–

USB 2.0 Interface

Pin Name	Pin #	I/O	Signal Description
HSD0+	53	I/O	USB 2.0 UFP Differential D+
HSD0–	54	I/O	USB 2.0 UFP Differential D–
HSD1+	7	I/O	USB 2.0 DFP1 Differential D+
HSD1–	8	I/O	USB 2.0 DFP1 Differential D–
HSD2+	74	I/O	USB 2.0 DFP2 Differential D+
HSD2–	75	I/O	USB 2.0 DFP2 Differential D–
HSD3+	65	I/O	USB 2.0 DFP3 Differential D+
HSD3–	66	I/O	USB 2.0 DFP3 Differential D–
HSD4+	16	I/O	USB 2.0 DFP4 Differential D+
HSD4–	17	I/O	USB 2.0 DFP4 Differential D–

Analog Command Block

Pin Name	Pin #	I/O	Signal Description
SSXI	55	I	25M Crystal Input
SSXO	56	O	25M Crystal Output
SSREXT	57	I	Connect to External Reference Resistor (6.04K+/- 1%)

Power and Ground

Pin Name	Pin #	I/O	Signal Description
GND	EPAD	GND	Ground
VCCD	9, 22, 46, 67	PWR	1.1V Core Power
VCC11	3, 12, 49, 61, 70	PWR	1.1V Analog Power
VCC11M	76	PWR	1.1V Analog Power
VCC33D	29, 43	PWR	3.3V Digital Power
VCC33	6, 15, 52, 64, 73	PWR	3.3V Analog Power
VCC33M	58	PWR	3.3V Analog Power
VCC5I	38	PWR	5-1.1V DC-DC Switching Regulator Input
LX	39	O	5-1.1V DC-DC Switching Regulator Output, Connect to Output Inductor (4.7uH) with Output Cap (10uF)
VCC11FB	40	I	5-1.1V DC-DC Switching Regulator Feedback
VCC5LDO	20	PWR	5-3.3V LDO Regulator Input
VCC33O	21	PWR	5-3.3V LDO Regulator Output Output Cap (4.7uF)

Test Pin

Pin Name	Pin #	I/O	Signal Description
TESTEN	23	I	Test Mode Enable Low: Normal mode. High: Test mode.
GPIO1/SMDAT	37	I/O	SMBus data with Proprietary Data Format. Open Drain. GPIO
GPIO2/SMCLK	36	I/O	SMBus clock with Proprietary Data Format. Open Drain. GPIO

Side Band Signal and Miscellaneous

Pin Name	Pin #	I/O	Signal Description
USBOC1	25	I	DFP USB OC (Gang mode) Open Drain (3.3V Max); Pin must be pulled high if NC. High: Normal Low: Hub DFP Over Current Event, Report Hub Over Current.
USBPE1	26	O	DFP USB PE (Gang mode) USB Power Enable Mode High: Enable Low: Off
GPIA	18	I	CDP Charging mode strapping: (Can't be floating) High: Enable CDP and Enable U1/U2 on DFP Low: Disable CDP on DFP
GPOA	19	O	GPO
NC5	41	-	Not use pin; can be floating.
GPOC	42	O	GPO
GPIB	27	I	U1/U2 strapping: (Can't be floating) High: Enable DFP U1/U2 support when CDP is disable. Low: Disable DFP U1/U2 support when CDP is disable.
GPOB	28	O	GPO
GPIOA	31	I/O	GPIO
GPIOB	30	I/O	GPIO
EXTPWRON	44	I	External Power Status (3.3V Max) High: External power attached Low: External power no detect
RESET#	24	I	System Reset Low: Reset High: Normal Operation
NC4	35	-	Not use pin; can be floating.
NC3	34	-	Not use pin; can be floating.
NC2	33	-	Not use pin; can be floating.
NC1	32	-	Not use pin; can be floating.
VBUSDET	45	I	UFP Vbus Detection (3.3V Max)

Electrical Specification

Absolute Maximum Rating

Symbol	Parameter	Min	Max	Unit	Note
T_{STG}	Storage Temperature	-40	125	°C	—
T_j	Junction Temperature	-	125	°C	—
VCC5LDO	5V Input Voltage	-0.5	5.5	V	—
VCC33O	3.3V Regulator Output Voltage	-0.5	3.63	V	—
VCC5I	5V Input Voltage	-0.5	5.5	V	—
V_{33}	3.3V Input Voltage	-0.5	3.63	V	—
V_{11}	1.1V Input Voltage	-0.5	1.26	V	—
V_{IN}	Input voltage at I/O pins	-0.5	(≦ 3.63) and (≦ V_{33}+0.3)	V	—
V_{ESD}	Electrostatic Discharge	-2000	2000	V	Human Body Model
θ_{jc}	Thermal resistance between junction and case	QFN76 For 2-layer PCB: 13.8 QFN76 For 4-layer PCB: 11.4		°C/W	2L & 4L PCB definitions follow JESD51-7
θ_{ja}	Thermal resistance between junction and ambient	QFN76 For 2-layer PCB: 59.1 QFN76 For 4-layer PCB: 24.6		°C/W	
P_D	Power dissipation	—	1	W	

Note1: Stress above conditions may cause permanent damage to the device.
Functional operation of this device should be restricted to the conditions described.
Note2: About thermal factors, T_a is the concerned ambient temperature, and
$\theta_{ca} = \theta_{ja} - \theta_{jc}$
$T_J = \theta_{ja} * P_D + T_a$
$T_c = \theta_{ca} * P_D + T_a$

Operating Conditions

Symbol	Parameter	Min	Max	Unit	Note
T_A	Ambient Temperature	0	70	°C	—
VCC5LDO	5V Input Voltage	4	5.25	V	—
VCC33O	3.3V Regulator Output Voltage	3.0	3.6	V	—
VCC5I	5V Input Voltage	4	5.25	V	—
V_{33}	3.3V Input Voltage	3.0	3.6	V	—
V_{11}	1.1V Input Voltage	1	1.2	V	—
V_{IL}	Input Low Voltage	—	0.8	V	—
V_{IH}	Input High Voltage	2.3	—	V	—
V_{OL}	Output Low Voltage	—	0.4	V	I_{OL}=4mA
V_{OH}	Output High Voltage	2.4	—	V	I_{OH}=4mA
I_{IL}	Input Leakage Current	—	+/-10	μA	$0<V_i<V_{33}$
I_{OZ}	Tristate Leakage Current	—	+/-20	μA	$0<V_o<V_{33}$

Power consumption

The following consumption value applies up to typical condition.

Device connection	Typical		Suspend	
	V_5(mA)	Power(mW)	V_5(mA)	Power(mW)
4 * SS	156	780	1.8	9
4 * HS	50.5	252.5	1.8	9
No Device	1.8	9	1.8	9

Note: $T_{A=25}$°C, Internal power solution (V11: 0.85V@Suspend).
SS: Super Speed (USB3.1 Gen1) Device
HS: High Speed (USB2.0) Device

General Reflow Profile Guidelines

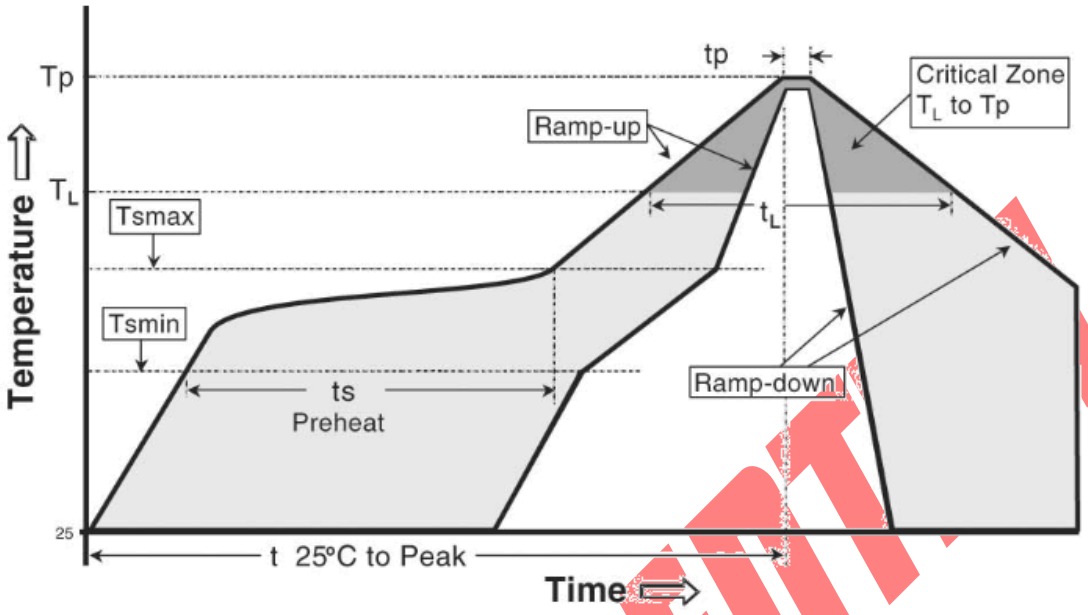


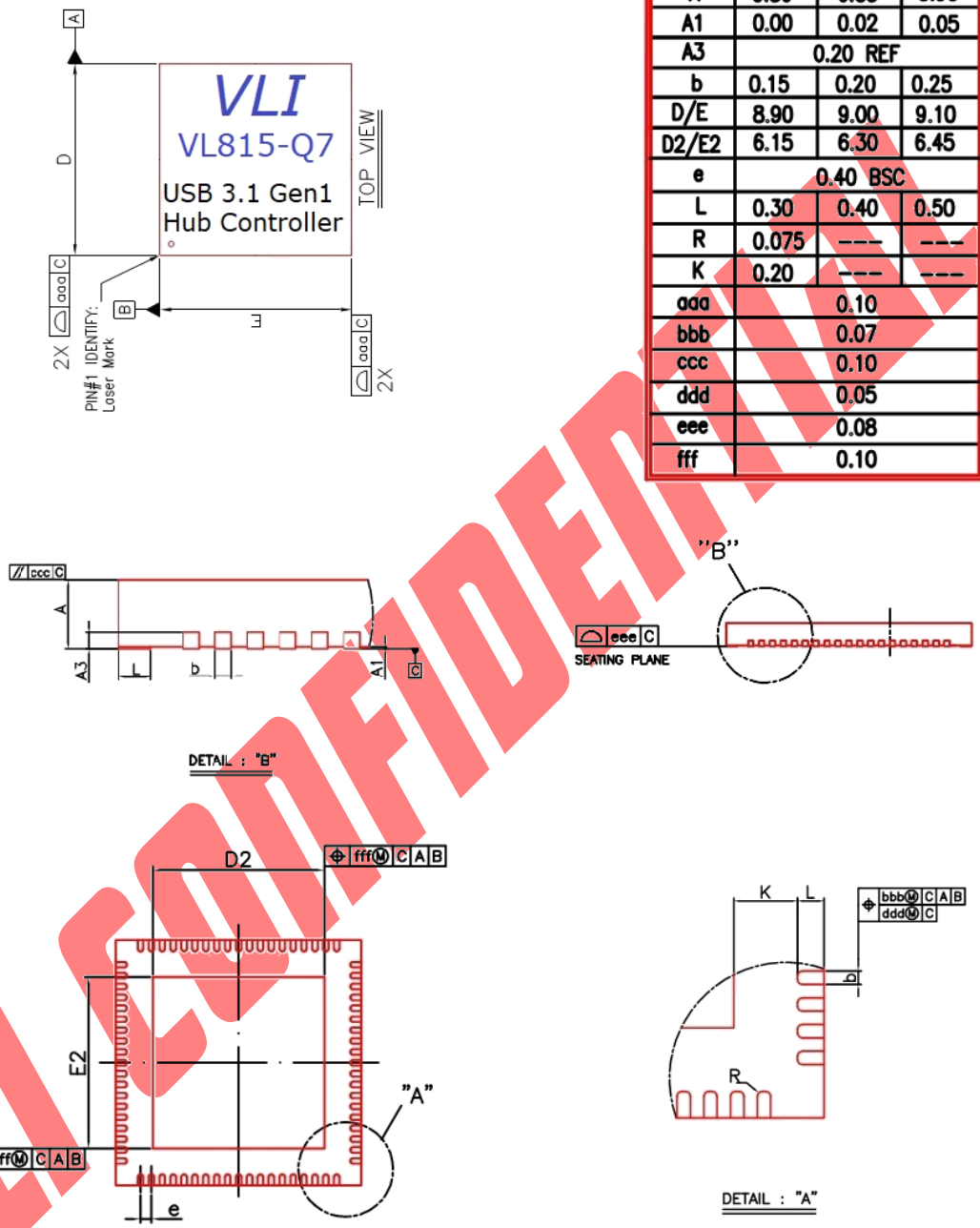
Figure 3 –Reflow

Profile Feature:	**Sn-Pb Eutectic**	**Pb-Free solder**
Average ramp-up rate (Liquidus Temperature (T_L) to Peak)	3°C/second max.	3°C/second max.
Preheat/Soak Temperature Min. (T_{smin}) Temperature Max. (T_{smax}) Time (min to max) (t_s)	 100°C 150°C 60-120 seconds	 150°C 200°C 60-120 seconds
Ts(max) to Tl -Ramp-up Rate		3°C/second max.
Time maintained above: Temperature (T_L) Time (t_L)	 183°C 60-150 seconds	 217°C 60-150 seconds
Peak package body temperature(Tp) Time within 5°C of actual peak temperature(Tp)	225+5/-0°C 20 seconds	255 +5/0°C 30 seconds
Ramp-down rate (T_p to T_L)	6°C/second max.	6°C/second max.
Time 25°C to peak temperature	6 minutes max.	8 minutes max.

***Note 1:** All temperatures refer to the center of package, measured on package body surface

***Note 2:** The reflow condition may vary with PCB design, pitch, size, reflow condition and solder suppliers, please contact your solder and reflow vendors.

Package Mechanical Specifications (VL815-Q7)



Symbol	Dimension in mm		
	MIN	NOM	MAX
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
A3		0.20 REF	
b	0.15	0.20	0.25
D/E	8.90	9.00	9.10
D2/E2	6.15	6.30	6.45
e		0.40 BSC	
L	0.30	0.40	0.50
R	0.075	---	---
K	0.20	---	---
aaa		0.10	
bbb		0.07	
ccc		0.10	
ddd		0.05	
eee		0.08	
fff		0.10	

Figure 4 – Mechanical Specification – QFN 76L 9x9x0.85 mm Package

Package Top Side Marking & Ordering Information

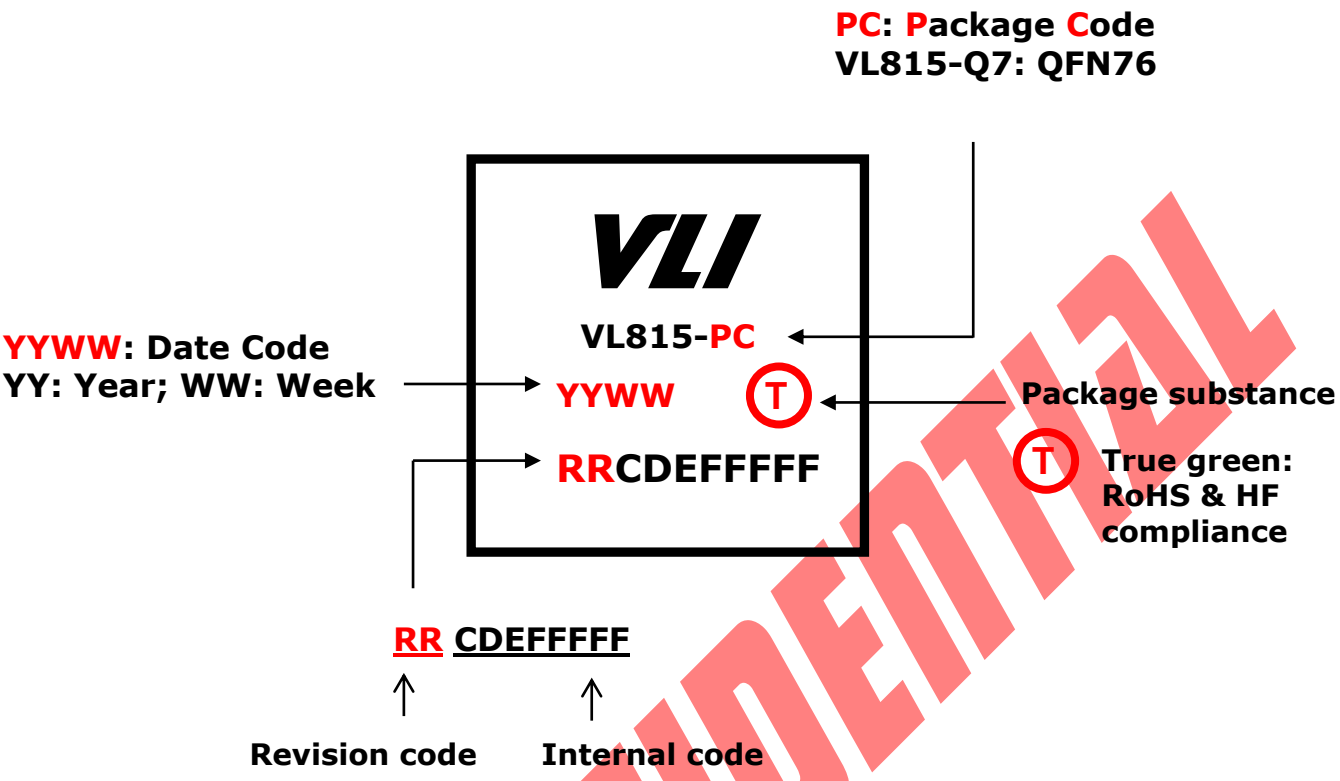


Figure 5 –Package Top Side Marking

Ordering Information

Please contact VIA Labs sales representative or distributor in your region for ordering part number details.

VIA Labs, Inc.
www.via-labs.com
7F, 529-1, Zhongzheng Rd.,
Xindian District, New Taipei City 23148 Taiwan, R.O.C.
TEL: (886-2) 2218-1838