LONTIUM SEMICONDUCTOR CORPORATION

ClearEdge™ Technology

LT8712EXI

Type-C/DP1.2 to HDMI2.0/VGA Converter

Datasheet

1. Features

- **USB Type-C**
  - Compliant with VESA DisplayPort Alt Mode on USB Type-C Standard V1.0
  - Compliant with USB Power Delivery Specification R2.0, V1.0
  - Compatible with USB Type-C Cable and Connector Specification R1.2
  - Built-in dual CC controllers for charger and normal communication
  - Flexible USB Type-C switching for USB3.0 5Gbps and DisplayPort Alt Mode up to 5.4Gbps
  - Compliant with HDMI 1.4b Alt Mode on USB Type-C Specification V1.0
- **DP1.2 Receiver**
  - Compliant with VESA DP1.2
  - Support 1.62/2.7/5.4Gbps
  - Support 1/2/4 lanes
  - Support SSC
  - 1Mbps AUX channel
  - Compliant with HDCP1.3
  - SST/MST mode
  - Adaptive receiver equalization for PCB, cable and connector losses
  - Support lane swap(arbitrarily) and polarity inversion(independent)
  - Receiver PHY is HDMI signal compatible
- **Dual HDMI2.0 Transmitters**
  - Compliant with HDMI2.0, HDMI1.4 and DVI1.0
  - Dual HDMI ports
  - Integrated one HDCP2.2 engine and one HDCP1.4 engine, each for one HDMI transmitter
  - Data rate up to 6Gbps
  - Support UHD 4k@60Hz(RGB and YCbCr 4:4:4)
  - Support TMDS scrambling for EMI/RFI reduction
  - Support SCDC(Status and Control Data Channel)
  - Support CEC
  - AC-couple capable
  - Support channel swap(arbitrarily) and polarity inversion(independent)
  - Programmable transmitter swing and pre-emphasis
  - Downstream receiver sensing
  - 5V tolerance DDC/HPD I/Os
- **Triple-Channel Video DAC**
  - Compliant with VESA VSIS1.2
  - 200MSPS throughput and WUXGA timing support
  - Support CSC(Color Space Conversion) between RGB and YCbCr 4:4:4, YCbCr 4:4:4 and YCbCr 4:2:2
  - Amplitude calibration
  - YPbPr output capable
  - R/B swappable
  - Support separate SYNC or embedded SYNC (SOG/SOY)
  - Load sensing
  - 5V tolerance DDC I/Os
- **Digital Audio Outputs**
  - I2S and SPDIF interface
  - 8-channel LPCM or compressed audio
  - Sample rate up to 192kHz
- **Miscellaneous**
  - DP receiver to HDMI transmitter bypass to support HDMI Alt Mode
  - Internal or external oscillator
  - Integrated microprocessor
  - Embedded SPI flash for firmware and HDCP keys
  - GPIOs for VBUS/VCONN/AUX and other system controls
  - Integrated 100/400kHz I2C slave
  - Firmware update through SPI, AUX or I2C interface
  - Low power consumption
  - Power supply: 3.3V for I/O and 1.2V for core
  - ESD 4kV HBM
  - Temperature Range: -40℃ ~ +85℃
  - Package: 128-pin QFN 14*14

2. General Description

The LT8712EXI is a high performance Type-C/DP1.2 to HDMI2.0/VGA converter, designed to connect a USB Type-C source or a DP1.2 source to a VGA sink and up to two HDMI2.0 sinks simultaneously. The LT8712EXI integrates a DP1.2 compliant receiver (MST capable), a high-speed triple-channel video DAC and two HDMI2.0 compliant transmitters. Also, two CC controllers are included for CC communication to implement DP Alt Mode and power delivery function, one for upstream Type-C port and another for downstream port. On-chip USB3.0 switch is a high-speed bi-directional passive switch which provides flexible switching to accommodate connector flipping. This switch also handles muxing between 2-ch data / 2-ch video and all 4-ch video.

The DP interface comprises 4 main lanes, AUX channel, and HPD signal. The receiver supports maximum 5.4Gbps (HBR2) data rate per lane and features multi-stream transporting (MST) which enables the transmission of 2 independent AV streams from a single DP link. The DP receiver incorporates HDCP 1.3 content protection scheme with embedded key for secure transmission of digital audio-video content.

The VGA interface consists of analog R/G/B video, HSYNC, VSYNC, and DDC signals. The 8-bit video DAC supports 200MSPS throughput which covers graphic resolutions from VGA (640x480) to WUXGA (1920x1200). Analog video signal amplitude ranges from 0 to 700mV and conforms to the VSIS 1.2 standards. The R and B channel can be swapped with each other to facilitate PCB trace routing. The analog video interface can also be configured to output YPbPr component video, with pins mapping to VGA G, B and R channel respectively. The interface supports separate SYNC and embedded SYNC (SOG/SOY). The video DAC also aids in monitor detection by performing load sensing, and calibrates its output amplitude automatically.

The HDMI interface includes 4 TMDS clock/data pairs, DDC, and HPD signal. The HDMI transmitter is capable of supporting up to 6Gpbs data rate, quite adequate for handling video resolutions up to FHD 1080p 120Hz 3D and UHD 4k 60Hz formats. The transmitter also performs downstream RX sensing in both DC and AC coupling applications. The LT8712EXI incorporates two HDMI transmitters and two HDCP engines which support HDCP1.4 and HDCP2.2 respectively, each for one HDMI transmitter. With the inclusion of HDCP, the LT8712EXI allows secure transmission of protected content. Embedded key is available that provides the highest level of HDCP key security.

The DP receiver PHY is HDMI signal compatible. It can receive HDMI signal and then bypass to any HDMI transmitter PHY or both simultaneously. This feature allows the LT8712EXI to suitably support HDMI Alt Mode. The integrated CC controller will handle DDC/CEC protocol conversion and communication.

Besides analog and digital video output interfaces, the LT8712EXI also provides digital audio output interfaces: I2S and SPDIF. The audio stream is extracted and recovered from DP data stream, and then routed to digital audio outputs or HDMI outputs. The device supports 8-channel LPCM or compressed audio at maximum 192kHz sample rate.

The device is capable of automatic operation which is enabled by an integrated microprocessor that uses an embedded SPI flash for firmware storage. System control is also available through the use of a dedicated configuration I2C slave interface.

The LT8712EXI is a 128-pin QFN package with ePad and specified over the -40℃ to +85℃ operating temperature range.

3. Applications

- Docking station
- Dongle
- Video hub

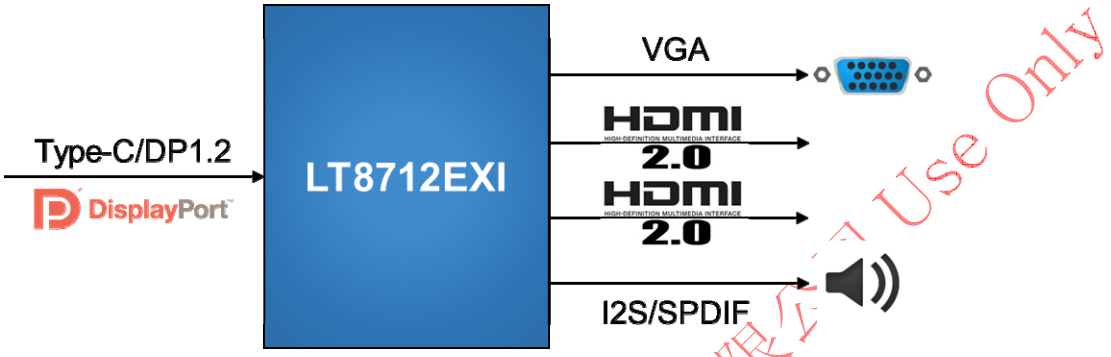

Figure 3.1 Application Diagram

4. Ordering Information

Table 4.1 Ordering Information

Part Number	Operating Temperature Range	Package	Packing Method
LT8712EXI	-40° C to +85° C	QFN128 (14*14)	Tray

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5. Revision History

Version	Owner	Content	Date
R1.0	HF X	Initial datasheet creation	12/14/2016
R1.1	HF X	Updated temperature data	12/21/2016
R1.2	HF X	Fixed typos	01/14/2017
R1.3	HF X	Updated package	04/25/2017
R1.4	PP J	Modify the format of the document	05/20/2017
R1.5	HF X	Added contents about USB switch for package LT8712EXI	09/12/2017
R1.6	HF X	Deleted LT8712EX relevant contents	12/26/2017
	N W	Update package information	11/15/2018
R1.7	HF X	Updated power consumption	01/22/2019
R1.8	PP J	Updated Figure 6.1.1	07/29/2019

6. Pinning Information

6.1 Pin Configuration

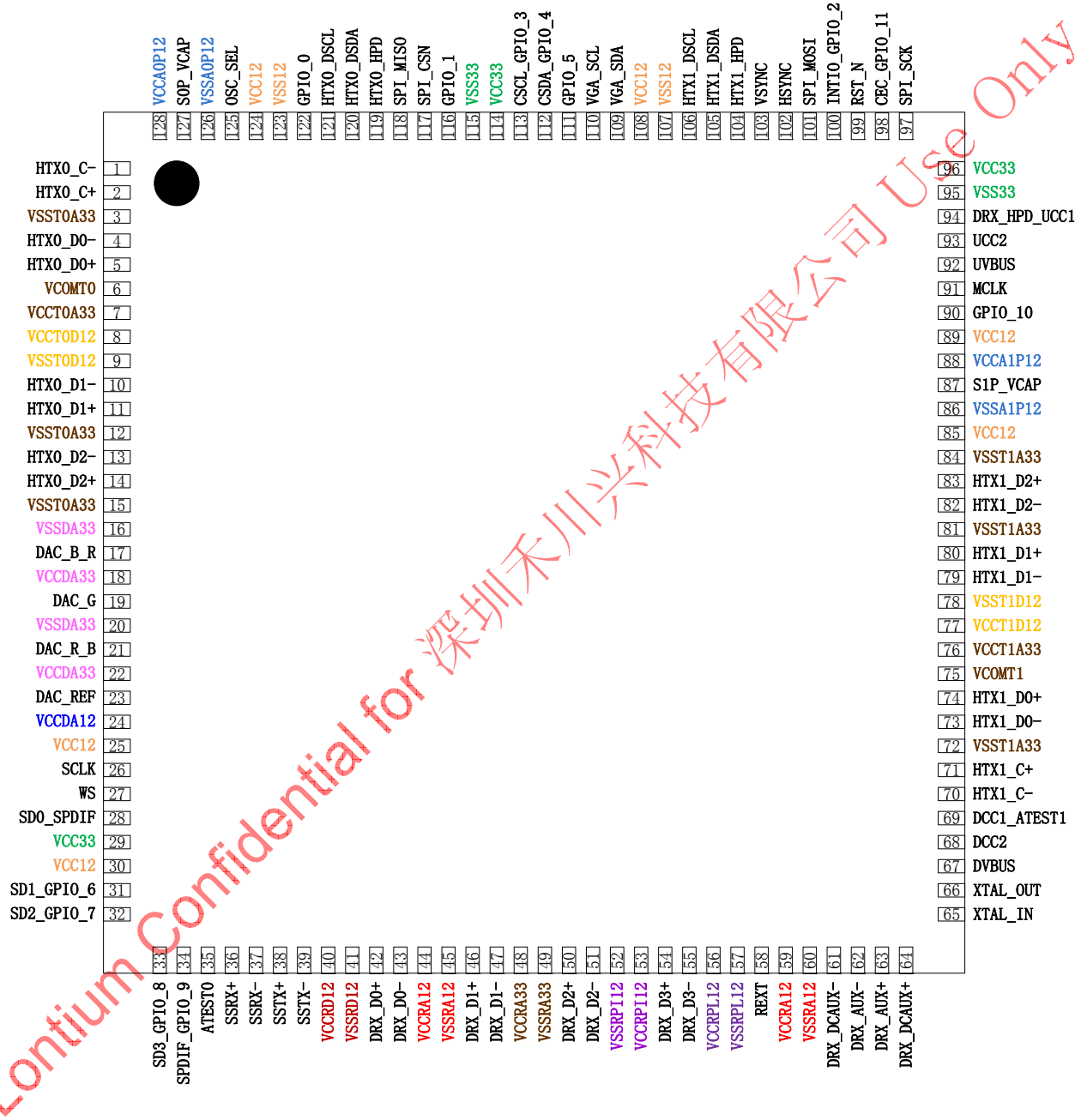


Figure 6.1.1 LT8712EXI QFN128 (14*14) Top View

6.2 Pin Description

Table 6.2.1 LT8712EXI Pin Description

Pin	Name	Function	Notes
1, 2, 4, 5, 10, 11, 13, 14	HTX0_C-, HTX0_C+, HTX0_D0-, HTX0_D0+, HTX0_D1-, HTX0_D1+, HTX0_D2-, HTX0_D2+	High speed output of HDMI TX port 0	AC-coupling capable
3, 12, 15	VSST0A33	Ground rail of 3.3V analog power for HDMI TX port 0	
6	VCOMT0	AC-couple biasing common ground for HDMI TX port 0	
7	VCCT0A33	Power rail of 3.3V analog power for HDMI TX port 0	
8	VCCT0D12	Power rail of 1.2V digital power for HDMI TX port 0. This power greatly impacts on jitter performance.	
9	VSST0D12	Ground rail of 1.2V digital power for HDMI TX port 0. This power greatly impacts on jitter performance.	
16, 20	VSSDA33	Ground rail of 3.3V analog power for video DAC	
17	DAC_B_R	Video DAC output, programmable B or R	
18, 22	VCCDA33	Power rail of 3.3V analog power for video DAC	
19	DAC_G	Video DAC G output	
21	DAC_R_B	Video DAC output, programmable R or B	
23	DAC_REF	Analog current reference for video DAC. A resistor of 4kΩ (1%) should tie this pin to VSSDA33.	
24	VCCDA12	Power rail of 1.2V digital power for video DAC	
25, 30, 85, 89, 108, 124	VCC12	Power rail of 1.2V digital core power	
26	SCLK	Audio I2S serial clock output	LVTTL, internal 100kΩ pull-down
27	WS	Audio I2S word selection output	LVTTL, internal 100kΩ pull-down
28	SD0_SPDIF	Audio I2S serial data 0 output which can also be configured as audio SPDIF output	LVTTL, internal 100kΩ pull-down
29, 96, 114	VCC33	Power rail of 3.3V LVTTL I/O power	
31	SD1_GPIO_6	Audio I2S serial data 1 output which can also be configured as general purpose I/O 6	LVTTL, internal 100kΩ pull-down
32	SD2_GPIO_7	Audio I2S serial data 2 output which can also be configured as general purpose I/O 7	LVTTL, internal 100kΩ pull-down
33	SD3_GPIO_8	Audio I2S serial data 3 output which can also be configured as general purpose I/O 8	LVTTL, internal 100kΩ pull-down
34	SPDIF_GPIO_9	Audio SPDIF output which can also be configured as general purpose I/O 9	LVTTL, internal 100kΩ pull-down

Pin	Name	Function	Notes
35	ATEST0	Analog test pin 0	Analog/LVTTL
36, 37, 38, 39	SSRX+, SSRX-, SSTX+, SSTX-	High speed data of USB3.0 port. SSRX+/SSRX- should be connected to USB3.0 RX, and SSTX+/SSTX- should be connected to USB3.0 TX.	
40	VCCRD12	Power rail of 1.2V digital power for DisplayPort RX. This power greatly impacts on RX performance.	
41	VSSRD12	Ground rail of 1.2V digital power for DisplayPort RX. This power greatly impacts on RX performance.	
42, 43, 46, 47, 50, 51, 54, 55	DRX_D0+, DRX_D0-, DRX_D1+, DRX_D1-, DRX_D2+, DRX_D2-, DRX_D3+, DRX_D3-	DisplayPort RX main link input	
44, 59	VCCRA12	Power rail of 1.2V analog power for DisplayPort RX	
45, 60	VSSRA12	Ground rail of 1.2V analog power for DisplayPort RX	
48	VCCRA33	Power rail of 3.3V analog power for DisplayPort RX	
49	VSSRA33	Ground rail of 3.3V analog power for DisplayPort RX	
52	VSSRPI12	Ground rail of 1.2V analog power for DisplayPort RX PI	
53	VCCRPI12	Power rail of 1.2V analog power for DisplayPort RX PI	
56	VCCRPL12	Power rail of 1.2V analog power for DisplayPort RX PLL	
57	VSSRPL12	Ground rail of 1.2V analog power for DisplayPort RX PLL	
58	REXT	Analog current reference. A resistor of 7.68kΩ (1%) should tie this pin to VSSRA33.	
61, 64	DRX_DCAUX-, DRX_DCAUX+	DisplayPort RX AUX interface(DC-coupled connection)	LVTTL, internal 1MΩ pull-up/-down
62, 63	DRX_AUX-, DRX_AUX+	DisplayPort RX AUX interface(AC-coupled connection)	
65, 66	XTAL_IN, XTAL_OUT	Crystal oscillator interface	LVTTL, 27MHz
67	DVBUS	VBUS detection for downstream USB Type-C port	Analog, 3.3V max
68	DCC2	CC2 pin for downstream USB Type-C port	
69	DCC1_ATEST1	CC1 pin for downstream USB Type-C port which can also be configured as analog test pin 1	ATEST1: analog/LVTTL, 5V tolerance
70, 71, 73, 74, 79, 80, 82, 83	HTX1_C-, HTX1_C+, HTX1_D0-, HTX1_D0+, HTX1_D1-, HTX1_D1+, HTX1_D2-, HTX1_D2+	High speed output of HDMI TX port 1	AC-coupling capable
72, 81, 84	VSST1A33	Ground rail of 3.3V analog power for HDMI TX port 1	
75	VCOMT1	AC-couple biasing common ground for HDMI TX port 1	
76	VCCT1A33	Power rail of 3.3V analog power for HDMI TX port 1	
77	VCCT1D12	Power rail of 1.2V digital power for HDMI TX port 1. This power greatly impacts on	

Pin	Name	Function	Notes
		jitter performance.	
78	VSST1D12	Ground rail of 1.2V digital power for HDMI TX port 1. This power greatly impacts on jitter performance.	
86	VSSA1P12	Ground rail of 1.2V analog power for audio stream 1 PLL	
87	S1P_VCAP	Decoupling capacitor connection for audio stream 1 PLL	
88	VCCA1P12	Power rail of 1.2V analog power for audio stream 1 PLL	
90	GPIO_10	General purpose I/O 10	LVTTL, internal 100kΩ pull-down
91	MCLK	Audio master clock output	LVTTL, internal 100kΩ pull-down
92	UVBUS	VBUS detection for upstream USB Type-C port	Analog, 3.3V max
93	UCC2	CC2 pin for upstream USB Type-C port	
94	DRX_HPD_UCC1	DisplayPort RX HPD output which can also be configured as CC1 pin for upstream USB Type-C port	DRX_HPD: LVTTL, 5V tolerance
95, 115	VSS33	Ground rail of 3.3V LVTTL I/O power	
97, 101, 117, 118	SPI_SCK, SPI_MOSI, SPI_CSN, SPI_MISO	Flash SPI programming interface	LVTTL, internal 100kΩ pull-down for SPI_SCK/SPI_MOSI/SPI_MISO and 100kΩ pull-up for SPI_CSN
98	CEC_GPIO_11	HDMI TX CEC pin which can also be configured as general purpose I/O 11	LVTTL/open-drain, optional internal 100kΩ pull-down
99	RST_N	Active low reset input	LVTTL, internal 100kΩ pull-up
100	INTIO_GPIO_2	Interrupt I/O which can also be configured as general purpose I/O 2	LVTTL, internal 100kΩ pull-down
102, 103	HSYNC, VSYNC	Horizontal/vertical synchronization output of VGA port	LVTTL, internal 100kΩ pull-up
104	HTX1_HPD	HPD input of HDMI TX port 1	LVTTL, 5V tolerance, internal 100kΩ pull-down
105, 106	HTX1_DSDA, HTX1_DSCL	DDC interface of HDMI TX port 1	LVTTL/open-drain, 5V tolerance, internal 100kΩ pull-up
107, 123	VSS12	Ground rail of 1.2V digital core power	
109, 110	VGA_SDA, VGA_SCL	DDC interface of VGA port	LVTTL/open-drain, 5V tolerance, internal 100kΩ pull-up

Pin	Name	Function	Notes
111	GPIO_5	General purpose I/O 5	LVTTL, internal 100kΩ pull-down
112, 113	CSDA_GPIO_4, CSCL_GPIO_3	Configuration I2C interface which can also be configured as general purpose I/O 4 and 3	LVTTL/open-drain, internal 100kΩ pull-up
116	GPIO_1	General purpose I/O 1	LVTTL, internal 100kΩ pull-down
119	HTX0_HPD	HPD input of HDMI TX port 0	LVTTL, 5V tolerance, internal 100kΩ pull-down
120, 121	HTX0_DSDA, HTX0_DSCL	DDC interface of HDMI TX port 0	LVTTL/open-drain, 5V tolerance, internal 100kΩ pull-up
122	GPIO_0	General purpose I/O 0	LVTTL, internal 100kΩ pull-down
125	OSC_SEL	Oscillator selection: 0 = using external oscillator; 1 = using internal or external oscillator is determined by register control.	LVTTL, internal 100kΩ pull-up
126	VSSA0P12	Ground rail of 1.2V analog power for audio stream 0 PLL	
127	S0P_VCAP	Decoupling capacitor connection for audio stream 0 PLL	
128	VCCA0P12	Power rail of 1.2V analog power for audio stream 0 PLL	

7. Function Block Diagram

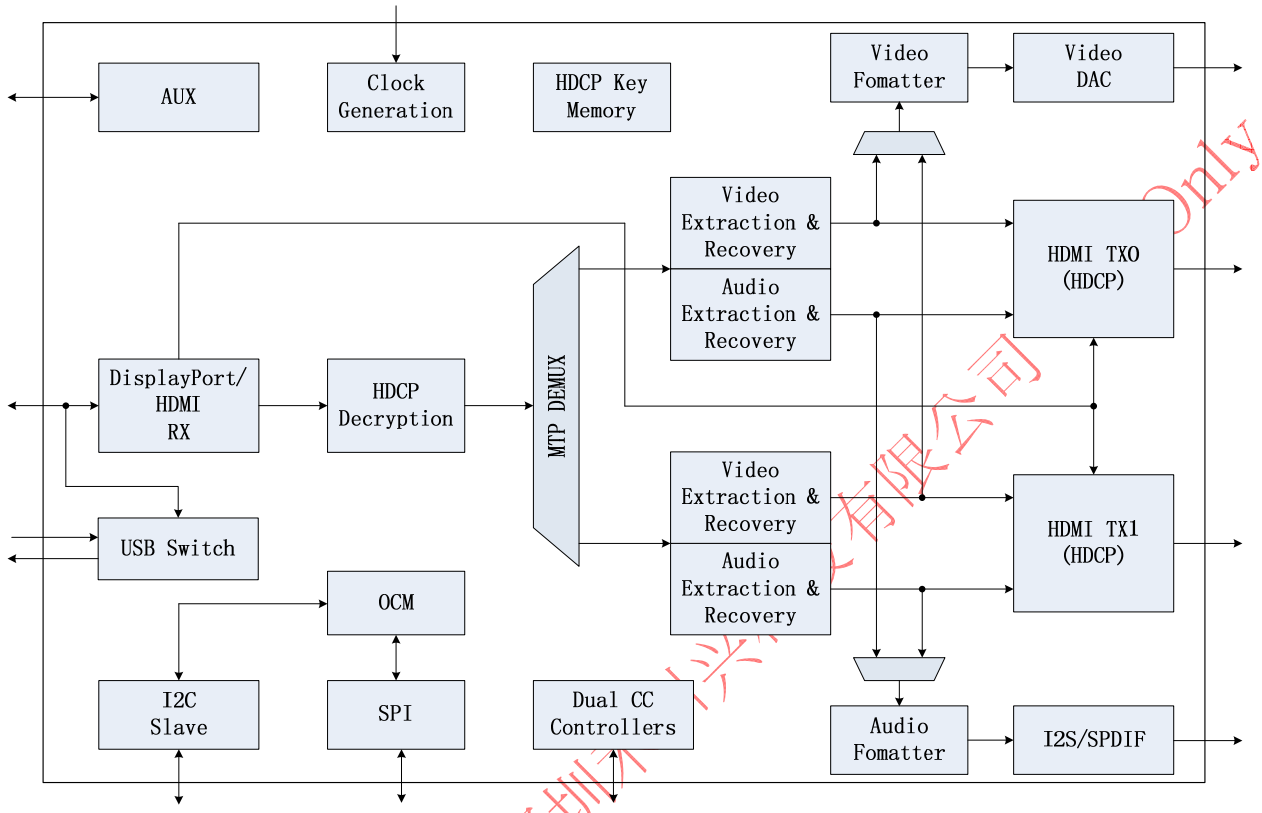


Figure 7.1 Function Block Diagram

8. Specification

8.1 Absolute Maximum Conditions

Table 8.1.1 Absolute Maximum Conditions

Symbol	Parameter	Min	Typ	Max	Units
VCC33 VCCRA33 VCCT0A33 VCCT1A33 VCCDA33	3.3V Power Supply	-0.3		4.0	V
VCC12 VCCRA12 VCCRD12 VCCRPL12 VCCRPI12 VCCT0D12 VCCT1D12 VCCA0P12 VCCA1P12 VCCDA12	1.2V Power Supply	-0.3		1.5	V
Vstg	Storage Temperature	-65		+150	℃
Tj	Junction Temperature			+150	℃

Notes:
1. Permanent device damage may occur if absolute maximum conditions are exceeded.
2. Function operation should be restricted to the conditions described under normal operating conditions.

8.2 Normal Operating Conditions

Table 8.2.1 Normal Operating Conditions

Parameter	Condition	Min	Typ	Max	Units
3.3V Power Supply	DC	3.0	3.3	3.6	V
1.2V Power Supply	DC	1.1	1.2	1.3	V
Supply-Noise Tolerance	DC to 500kHz			100	mVp-p
Ambient Temperature		-40		+85	℃
DP Main Link Receiver					
Unit Interval	HBR2		185		ps
Unit Interval	HBR		370		ps
Unit Interval	RBR		617		ps
SSC Down-spreading		0		0.5	%
SSC Modulation Frequency		30		33	kHz
Minimum Receiver Eye Width	at input pins	0.25			UI
Lane Intra-Pair Skew Tolerance	HBR2			50	ps
Lane Intra-Pair Skew Tolerance	HBR			60	ps
Lane Intra-Pair Skew Tolerance	RBR			260	ps
Lane-to-Lane Skew	at input pins			5700	ps
Differential Eye Voltage	at input pins	100		1320	mVp-p

Termination DC Resistance	Single-ended	45	50	55	Ω
DP AUX Channel					
Unit Interval		0.4	0.5	0.6	us
Differential Voltage	Transmitting	390		1380	mVp-p
Differential Voltage	Receiving	320		1360	mVp-p
Common-Mode Voltage		0		2	V
Termination DC resistance	Single-ended	45	50	55	Ω
Short-Circuit Current	Short to ground		30		mA
AC-Coupling Capacitor		75		200	nF
HDMI Transmitter					
Differential Output-Voltage Swing	50 ohm load	800	1000	1200	mVp-p
Output-Voltage High	Single-ended, 50 ohm load		VCCTxA33		V
Output-Voltage Low	Single-ended, 50 ohm load	VCCTxA33-0.6		VCCTxA33-0.4	V
Output Voltage During Power-Down	Single-ended, 50 ohm load	VCCTxA33-0.01		VCCTxA33+0.01	V
Common-Mode Output Voltage	Single-ended, 50 ohm load	VCCTxA33-0.3		VCCTxA33-0.2	V
Rise /Fall Time	20% to 80%	37.5	100	166	ps
DAC					
Resolution			8		bit
Clock Frequency				200	MHz
Output Current Variation	DAC-to-DAC			4	%
Integral Non-Linearity		-1	±0.5	+1	LSB
Differential Non-Linearity		-1	±0.5	+1	LSB
Output Amplitude	37.5 ohm load	0		770	mV
LVTTL Control and Status Interface					
LVTTL Input High Voltage		2.0			V
LVTTL Input Low Voltage				0.8	V
LVTTL Input Hysteresis		200			mV
LVTTL Output High Voltage		2.4			V
LVTTL Output Low Voltage				0.4	V
Open-Drain Output Low Voltage	R_{LOAD} 2kΩ to VCC33			0.4	V
Open-Drain Output Sink Current				5	mA
Supply Current					
HBR2, 4-lane, 4k60Hz*1	3.3V		76		mA
	1.2V		577		mA
HBR, 2-lane, 1080p60Hz*2	3.3V		90		mA
	1.2V		261		mA

8.3 Power-up Sequence

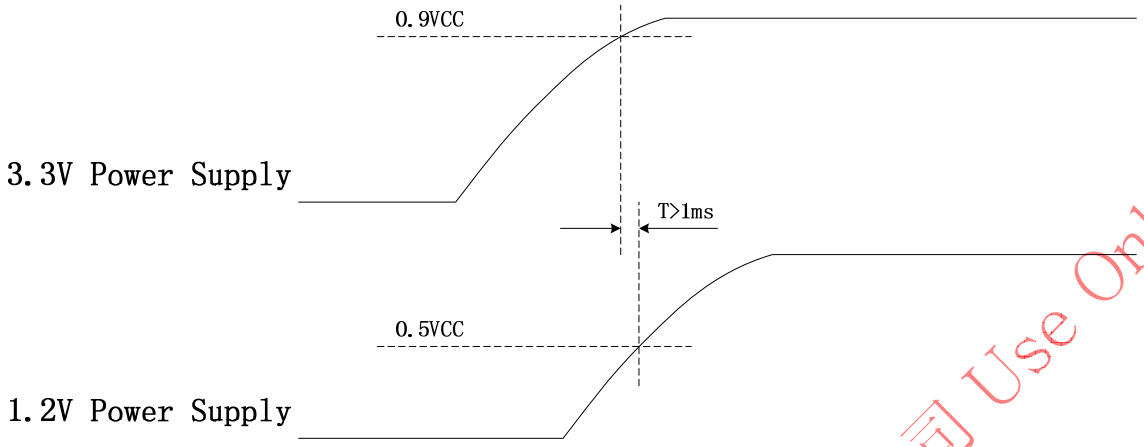


Figure 8.3.1 Power-up Sequence

9. Packaging

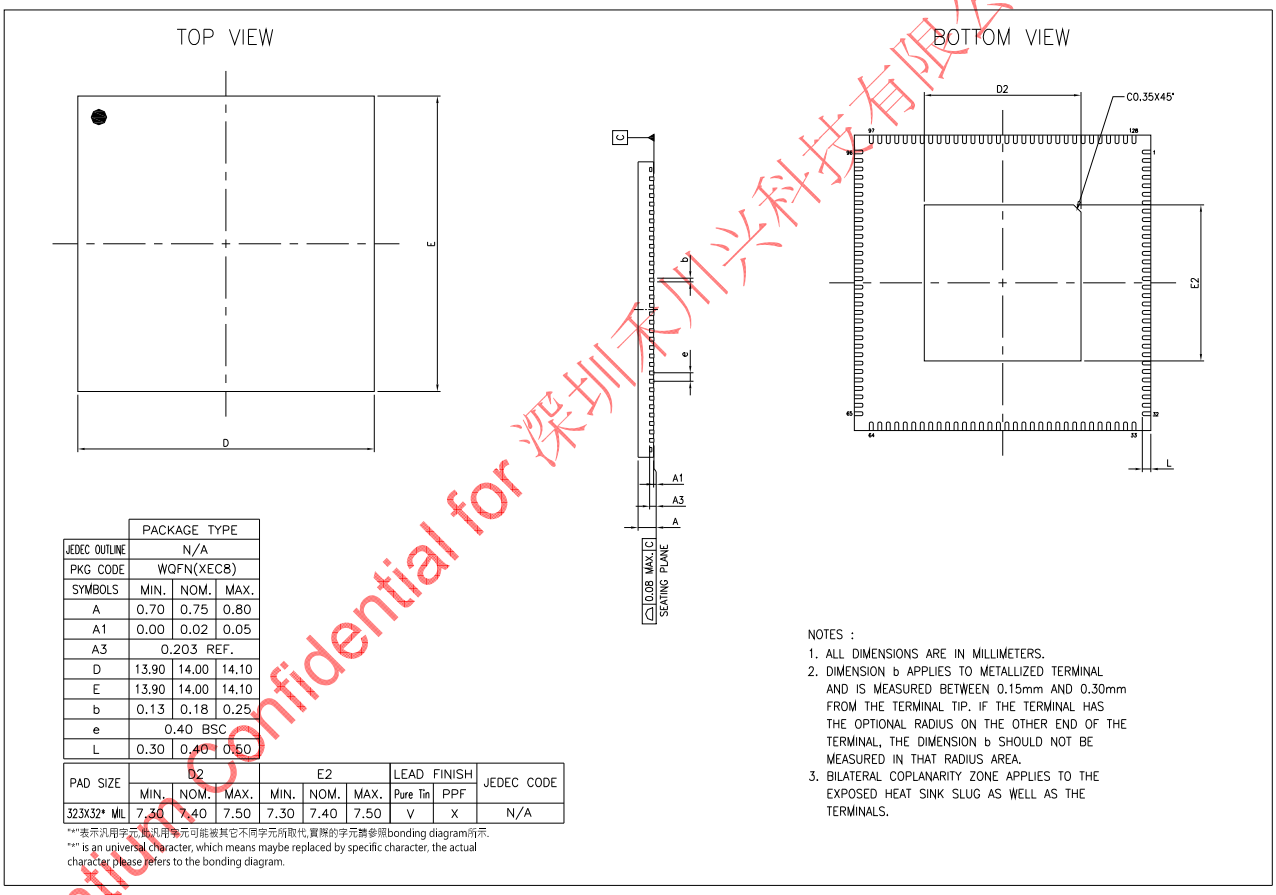
9.1 ePad Enhancement

The LT8712EXI is a 128-pin QFN package with ePad.

The ePad needs to be soldered to the PCB. The information in the following paragraphs is provided for applications which solder the ePad to the PCB.

The ePad must not be electrically connected to any other voltage level except ground (GND). A clearance of at least 0.25mm should be designed on the PCB between the edge of the ePad and the inner edges of the lead pads to avoid any electrical shorts.

9.2 Package Dimensions



	PACKAGE TYPE		
JEDEC OUTLINE	N/A		
PKG CODE	WQFN(XEC8)		
SYMBOLS	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3	0.203 REF.		
D	13.90	14.00	14.10
E	13.90	14.00	14.10
b	0.13	0.18	0.25
e	0.40 BSC		
L	0.30	0.40	0.50

PAD SIZE	D2			E2			LEAD FINISH		JEDEC CODE
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	Pure Tin	PPF	
323X32* MIL	7.30	7.40	7.50	7.30	7.40	7.50	V	X	N/A

*"表示汎用字元,該汎用字元可能被其它不同字元所取代,實際的字元請參照bonding diagram所示.
"*" is an universal character, which means maybe replaced by specific character, the actual character please refers to the bonding diagram.

Figure 9.2.1 LT8712EXI Package Dimensions

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Technical support: support@lontium.com
Sales: sales@lontium.com