LONTIUM SEMICONDUCTOR CORPORATION

ClearEdge™ Technology

LT8711EH-C

Type-C/DP1.2 to HDMI2.0 Converter

Datasheet

1. Features

- **USB Type-C**
  - Compliant with VESA DisplayPort Alt Mode on USB Type-C Standard V1.0
  - Compliant with USB Power Delivery Specification R2.0, V1.0
  - Compatible with USB Type-C Cable and Connector Specification R1.2
  - Built-in dual CC controllers for charger and normal communication
  - Compliant with HDMI 1.4b Alt Mode on USB Type-C Specification V1.0
- **DP1.2 Receiver**
  - Compliant with VESA DP1.2
  - Support 1.62/2.7/5.4Gbps
  - Support 1/2/4 lanes
  - Support SSC
  - 1Mbps AUX channel
  - Compliant with HDCP1.3
  - Adaptive receiver equalization for PCB, cable and connector losses
  - Support lane swap(arbitrarily) and polarity inversion(independent)
  - Receiver PHY is HDMI signal compatible
- **HDMI2.0 Transmitter**
  - Compliant with HDMI2.0, HDMI1.4 and DVI1.0
  - Compliant with HDCP2.2 and HDCP1.4
  - IData rate up to 6Gbps
  - Support UHD 4k@60Hz(RGB and YCbCr 4:4:4)
  - Support TMDS scrambling for EMI/RFI reduction
  - Support SCDC(Status and Control Data Channel)
  - AC-couple capable
  - Support channel swap(arbitrarily) and polarity inversion(independent)
  - Programmable transmitter swing and pre-emphasis
  - Downstream receiver sensing
  - 5V tolerance DDC/HPD I/Os
- **Miscellaneous**
  - DP receiver to HDMI transmitter bypass to support HDMI Alt Mode
  - Internal or external oscillator
  - Integrated microprocessor
  - Embedded SPI flash for firmware and HDCP keys
  - GPIOs for VBUS/VCONN/AUX and other system controls
  - Integrated 100/400kHz I2C slave
  - Firmware update through SPI, AUX or I2C interface
  - Low power consumption
  - Power supply: 3.3V for I/O and 1.2V for core
  - ESD 4kV HBM
  - Temperature Range: -40℃ ~ +85℃
  - 64-pin QFN 7.5*7.5 package

2. General Description

The LT8711EH-C is a high performance Type-C/DP1.2 to HDMI2.0 converter, designed to connect a USB Type-C source or a DP1.2 source to an HDMI2.0 sink. The LT8711EH-C integrates a DP1.2 compliant receiver, and an HDMI2.0 compliant transmitter. Also, two CC controllers are included for CC communication to implement DP Alt Mode and power delivery function, one for upstream Type-C port and another for downstream port.

The DP interface comprises 4 main lanes, AUX channel, and HPD signal. The receiver supports maximum 5.4Gbps (HBR2) data rate per lane. The DP receiver incorporates HDCP 1.3 content protection scheme with embedded key for secure transmission of digital audio-video content.

The HDMI interface includes 4 TMDS clock/data pairs, DDC, and HPD signal. The HDMI transmitter is capable of supporting up to 6Gpbs data rate, quite adequate for handling video resolutions up to FHD 1080p 120Hz 3D and UHD 4k 60Hz formats. The transmitter performs downstream RX sensing in both DC and AC coupling applications. The HDMI transmitter incorporates HDCP engines which support both HDCP1.4 and HDCP2.2. With the inclusion of HDCP, the LT8711EH-C allows secure transmission of protected content. Embedded key is available that provides the highest level of HDCP key security.

The DP receiver PHY is HDMI signal compatible. It can receive HDMI signal and then bypass to the HDMI transmitter PHY. This feature allows the LT8711EH-C to

suitably support HDMI Alt Mode. The integrated CC controller will handle DDC/CEC protocol conversion and communication.

The device is capable of automatic operation which is enabled by an integrated microprocessor that uses an embedded SPI flash for firmware storage. System control is also available through the use of a dedicated configuration I2C slave interface.

The LT8711EH-C is offered in a 64-lead QFN packages with ePad and is specified over the -40℃ to +85℃ operating temperature range.

3. Applications

- Docking station
- Dongle

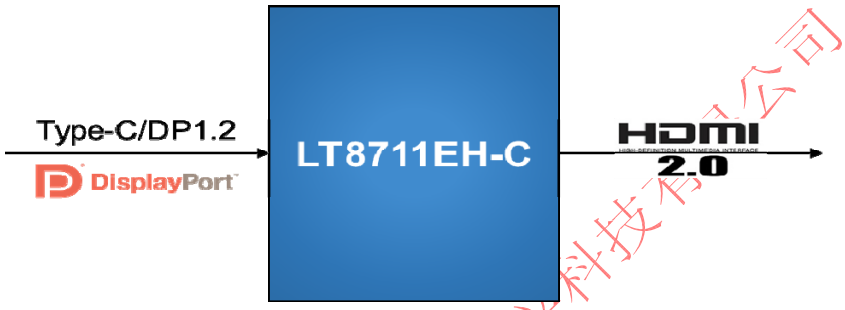


Figure 3.1 Application Diagram

4. Ordering Information

Table 4.1 Ordering Information

Part Number	Operating Temperature Range	Package	Packing Method
LT8711EH-C	-40℃ to +85℃	QFN64 (7.5*7.5)	Tray
LT8711EH-C-AU	-40℃ to +85℃	QFN64 (7.5*7.5)	Tray

Note: The suffix -AU denotes that it is an automotive grade device which is qualified by AEC-Q100 grade 3 testing.

Table of Contents

5. Revision History

Version	Owner	Content	Date
R1.0	HF X	Initial datasheet creation	01/07/2017
R1.1	PP J	Modify the format of the document	05/04/2017
R1.2	HF X	Updated power consumption	07/14/2017
	N W	Updated package information	11/15/2018
R1.3	HF X	Removed description of LT8711EH-CI	12/03/2018
R1.4	HF X	Added automotive version	05/23/2019
R1.5	PP J	Updated Figure 6.1.1	07/25/2019

6. Pinning Information

6.1 Pin Configuration

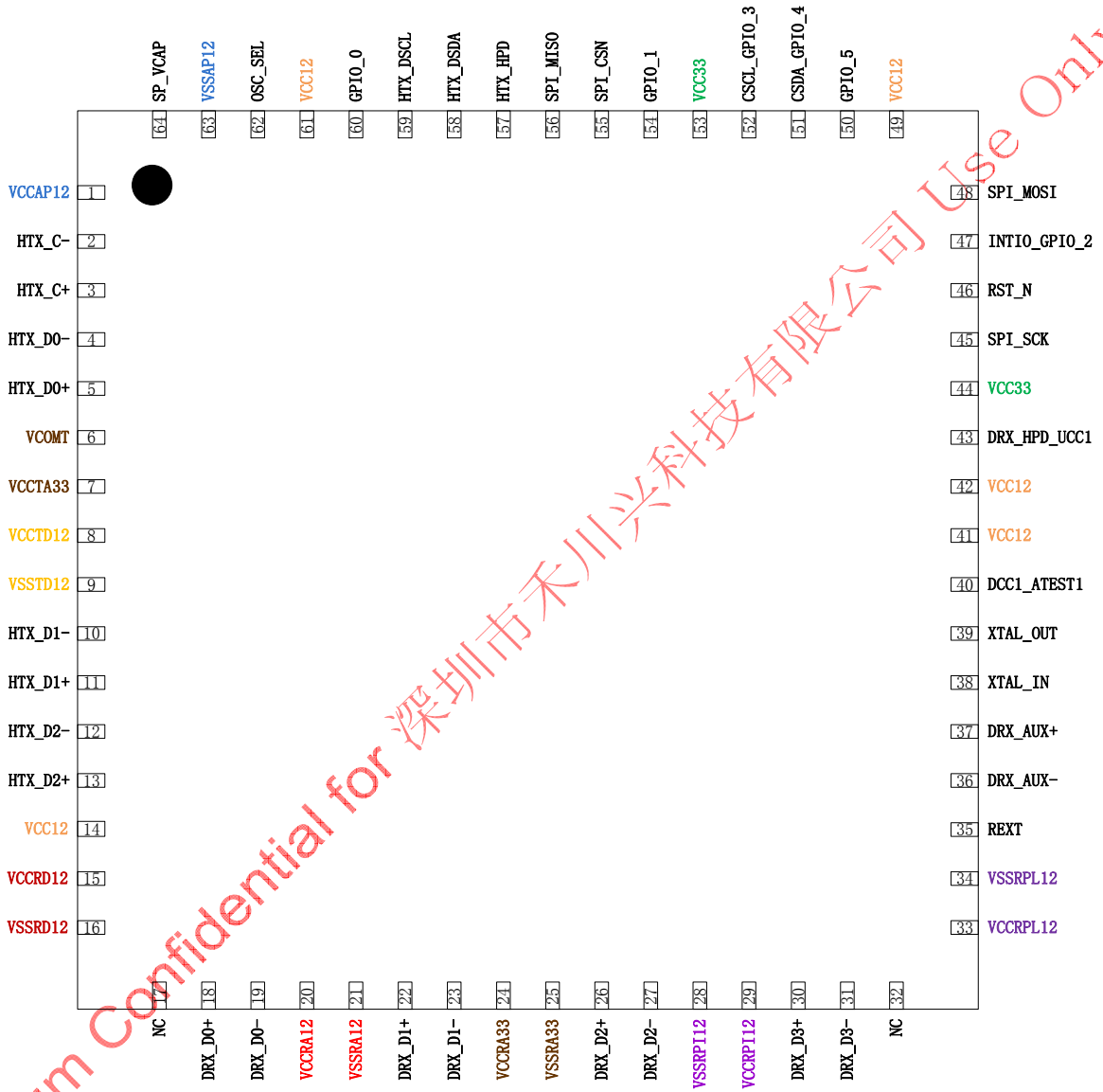


Figure 6.1.1 LT8711EH-C QFN64 (7.5*7.5) Top View

6.2 Pin Description

Table 6.2.1 LT8711EH-C Pin Description

Pin	Name	Function	Notes
1	VCCAP12	Power rail of 1.2V analog power for audio stream PLL	
2, 3, 4, 5, 10, 11, 12, 13	HTX_C-, HTX_C+, HTX_D0-, HTX_D0+, HTX_D1-, HTX_D1+, HTX_D2-, HTX_D2+	High speed output of HDMI TX	AC-coupling capable
6	VCOMT	AC-couple biasing common ground for HDMI TX	
7	VCCTA33	Power rail of 3.3V analog power for HDMI TX	
8	VCCTD12	Power rail of 1.2V digital power for HDMI TX. This power greatly impacts on jitter performance.	
9	VSSTD12	Ground rail of 1.2V digital power for HDMI TX. This power greatly impacts on jitter performance.	
14, 41, 42, 49, 61	VCC12	Power rail of 1.2V digital core power	
15	VCCRD12	Power rail of 1.2V digital power for DisplayPort RX. This power greatly impacts on RX performance.	
16	VSSRD12	Ground rail of 1.2V digital power for DisplayPort RX. This power greatly impacts on RX performance.	
17, 32	NC	No connection	
18, 19, 22, 23, 26, 27, 30, 31	DRX_D0+, DRX_D0-, DRX_D1+, DRX_D1-, DRX_D2+, DRX_D2-, DRX_D3+, DRX_D3-	DisplayPort RX main link input	
20	VCCRA12	Power rail of 1.2V analog power for DisplayPort RX	
21	VSSRA12	Ground rail of 1.2V analog power for DisplayPort RX	
24	VCCRA33	Power rail of 3.3V analog power for DisplayPort RX	
25	VSSRA33	Ground rail of 3.3V analog power for DisplayPort RX	
28	VSSRPI12	Ground rail of 1.2V analog power for DisplayPort RX PI	
29	VCCRPI12	Power rail of 1.2V analog power for DisplayPort RX PI	
33	VCCRPL12	Power rail of 1.2V analog power for DisplayPort RX PLL	
34	VSSRPL12	Ground rail of 1.2V analog power for DisplayPort RX PLL	
35	REXT	Analog current reference. A resistor of 7.68kΩ (1%) should tie this pin to VSSRA33.	
36, 37	DRX_AUX-, DRX_AUX+	DisplayPort RX AUX interface(AC-coupled connection)	
38, 39	XTAL_IN, XTAL_OUT	Crystal oscillator interface	LVTTL, 27MHz
40	DCC1_ATEST1	CC1 pin for downstream USB Type-C port which can also be configured as analog test pin 1	ATEST1: analog/LVTTL, 5V tolerance

Pin	Name	Function	Notes
43	DRX_HPD_UCC1	DisplayPort RX HPD output which can also be configured as CC1 pin for upstream USB Type-C port	DRX_HPD: LVTTL, 5V tolerance
44, 53	VCC33	Power rail of 3.3V LVTTL I/O power	
45, 48, 55, 56	SPI_SCK, SPI_MOSI, SPI_CSN, SPI_MISO	Flash SPI programming interface	LVTTL, internal 100kΩ pull-down for SPI_SCK/SPI_MOSI/SPI_MISO and 100kΩ pull-up for SPI_CSN
46	RST_N	Active low reset input	LVTTL, internal 100kΩ pull-up
47	INTIO_GPIO_2	Interrupt I/O which can also be configured as general purpose I/O 2	LVTTL, internal 100kΩ pull-down
50	GPIO_5	General purpose I/O 5	LVTTL, internal 100kΩ pull-down
51, 52	CSDA_GPIO_4, CSCL_GPIO_3	Configuration I2C interface which can also be configured as general purpose I/O 4 and 3	LVTTL/open-drain, internal 100kΩ pull-up
54	GPIO_1	General purpose I/O 1	LVTTL, internal 100kΩ pull-down
57	HTX_HPD	HPD input of HDMI TX	LVTTL, 5V tolerance, internal 100kΩ pull-down
58, 59	HTX_DSDA, HTX_DSCL	DDC interface of HDMI TX	LVTTL/open-drain, 5V tolerance, internal 100kΩ pull-up
60	GPIO_0	General purpose I/O 0	LVTTL, internal 100kΩ pull-down
62	OSC_SEL	Oscillator selection: 0 = using external oscillator; 1 = using internal or external oscillator is determined by register control.	LVTTL, internal 100kΩ pull-up
63	VSSAP12	Ground rail of 1.2V analog power for audio stream PLL	
64	SP_VCAP	Decoupling capacitor connection for audio stream PLL	
65	EPAD	Common ground	

7. Function Block Diagram

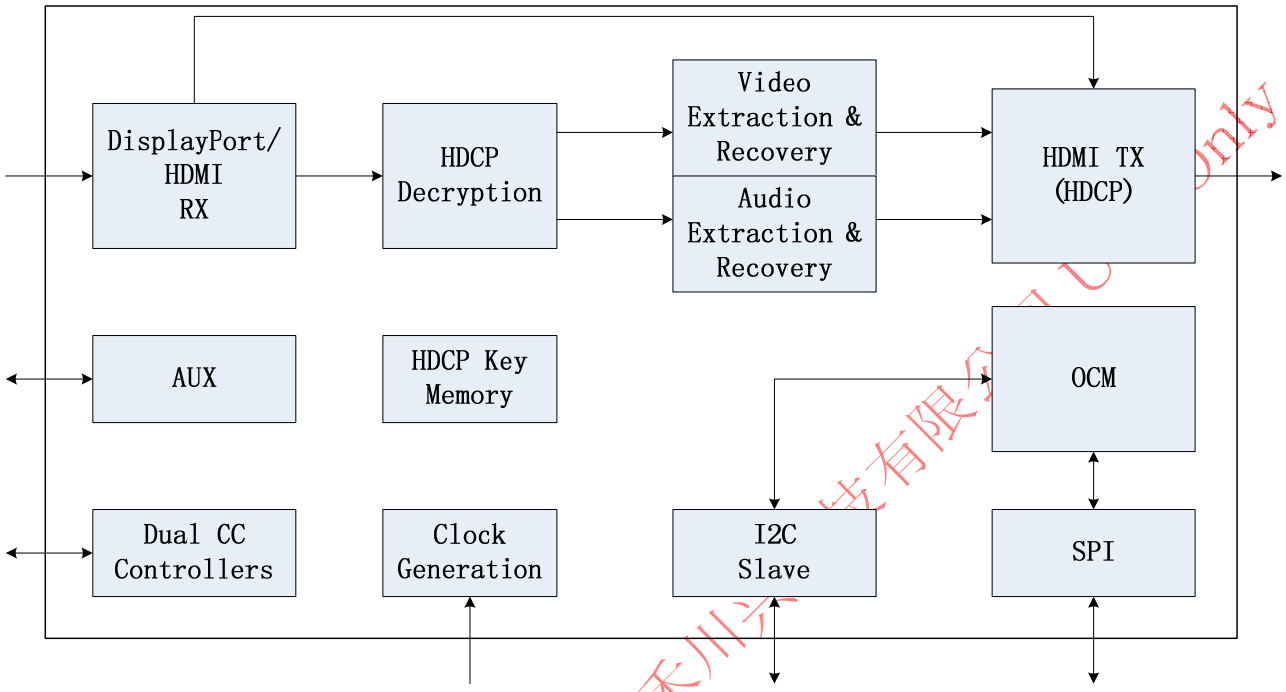


Figure 7.1 Function Block Diagram

8. Specification

8.1 Absolute Maximum Conditions

Table 8.1.1 Absolute Maximum Conditions

Symbol	Parameter	Min	Typ	Max	Units
VCC33 VCCRA33 VCCTA33	3.3V Power Supply	-0.3		4.0	V
VCC12 VCCRA12 VCCRD12 VCCRPL12 VCCRPI12 VCCTD12 VCCAP12	1.2V Power Supply	-0.3		1.5	V
Vstg	Storage Temperature	-65		+150	℃
Tj	Junction Temperature			+150	℃

Notes:
1. Permanent device damage may occur if absolute maximum conditions are exceeded.
2. Function operation should be restricted to the conditions described under normal operating conditions.

8.2 Normal Operating Conditions

Table 8.2.1 Normal Operating Conditions

Parameter	Condition	Min	Typ	Max	Units
3.3V Power Supply	DC	3.0	3.3	3.6	V
1.2V Power Supply	DC	1.1	1.2	1.3	V
Supply-Noise Tolerance	DC to 500kHz			100	mVp-p
Ambient Temperature		-40		+85	℃
DP Main Link Receiver					
Unit Interval	HBR2		185		ps
Unit Interval	HBR		370		ps
Unit Interval	RBR		617		ps
SSC Down-spreading		0		0.5	%
SSC Modulation Frequency		30		33	kHz
Minimum Receiver Eye Width	at input pins	0.25			UI
Lane Intra-Pair Skew Tolerance	HBR2			50	ps
Lane Intra-Pair Skew Tolerance	HBR			60	ps
Lane Intra-Pair Skew Tolerance	RBR			260	ps
Lane-to-Lane Skew	at input pins			5700	ps
Differential Eye Voltage	at input pins	100		1320	mVp-p
Termination DC Resistance	Single-ended	45	50	55	Ω
DP AUX Channel					
Unit Interval		0.4	0.5	0.6	us
Differential Voltage	Transmitting	390		1380	mVp-p

Differential Voltage	Receiving	320		1360	mVp-p
Common-Mode Voltage		0		2	V
Termination DC resistance	Single-ended	45	50	55	Ω
Short-Circuit Current	Short to ground			30	mA
AC-Coupling Capacitor		75		200	nF
HDMI Transmitter					
Differential Output-Voltage Swing	50 ohm load	800	1000	1200	mVp-p
Output-Voltage High	Single-ended, 50 ohm load	VCCTxA33			V
Output-Voltage Low	Single-ended, 50 ohm load	VCCTxA33-0.6		VCCTxA33-0.4	V
Output Voltage During Power-Down	Single-ended, 50 ohm load	VCCTxA33-0.01		VCCTxA33+0.01	V
Common-Mode Output Voltage	Single-ended, 50 ohm load	VCCTxA33-0.3		VCCTxA33-0.2	V
Rise /Fall Time	20% to 80%	37.5	100	166	ps
LVTTL Control and Status Interface					
LVTTL Input High Voltage		2.0			V
LVTTL Input Low Voltage				0.8	V
LVTTL Input Hysteresis		200			mV
LVTTL Output High Voltage		2.4			V
LVTTL Output Low Voltage				0.4	V
Open-Drain Output Low Voltage	R_{LOAD} 2kΩ to VCC33			0.4	V
Open-Drain Output Sink Current				5	mA
Supply Current					
Normal operation: HBR2, 4-lane, 2160p@60Hz	3.3V	76			mA
	1.2V	770			mA
Normal operation: HBR2, 4-lane, 2160p@30Hz	3.3V	76			mA
	1.2V	521			mA

8.3 Power-up Sequence

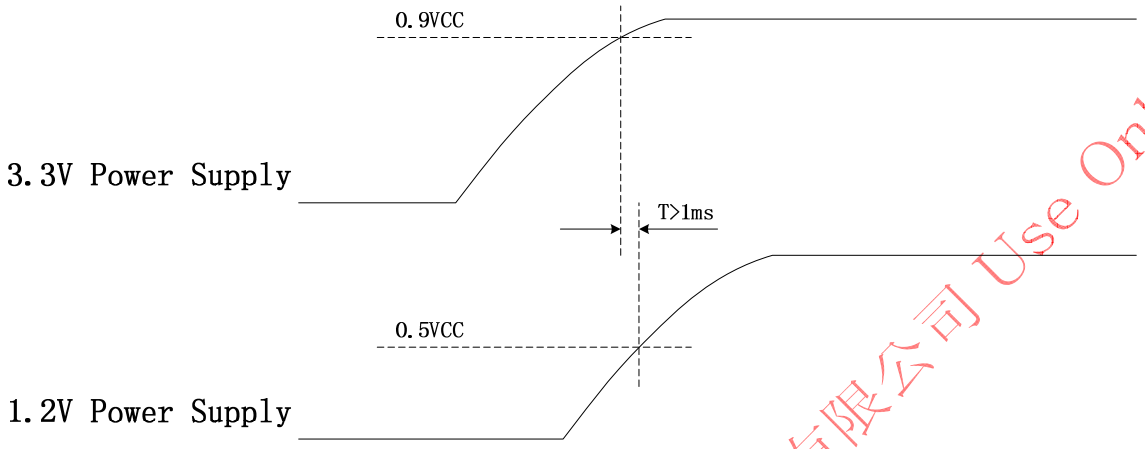


Figure 8.3.1 Power-up Sequence

9. Package Information

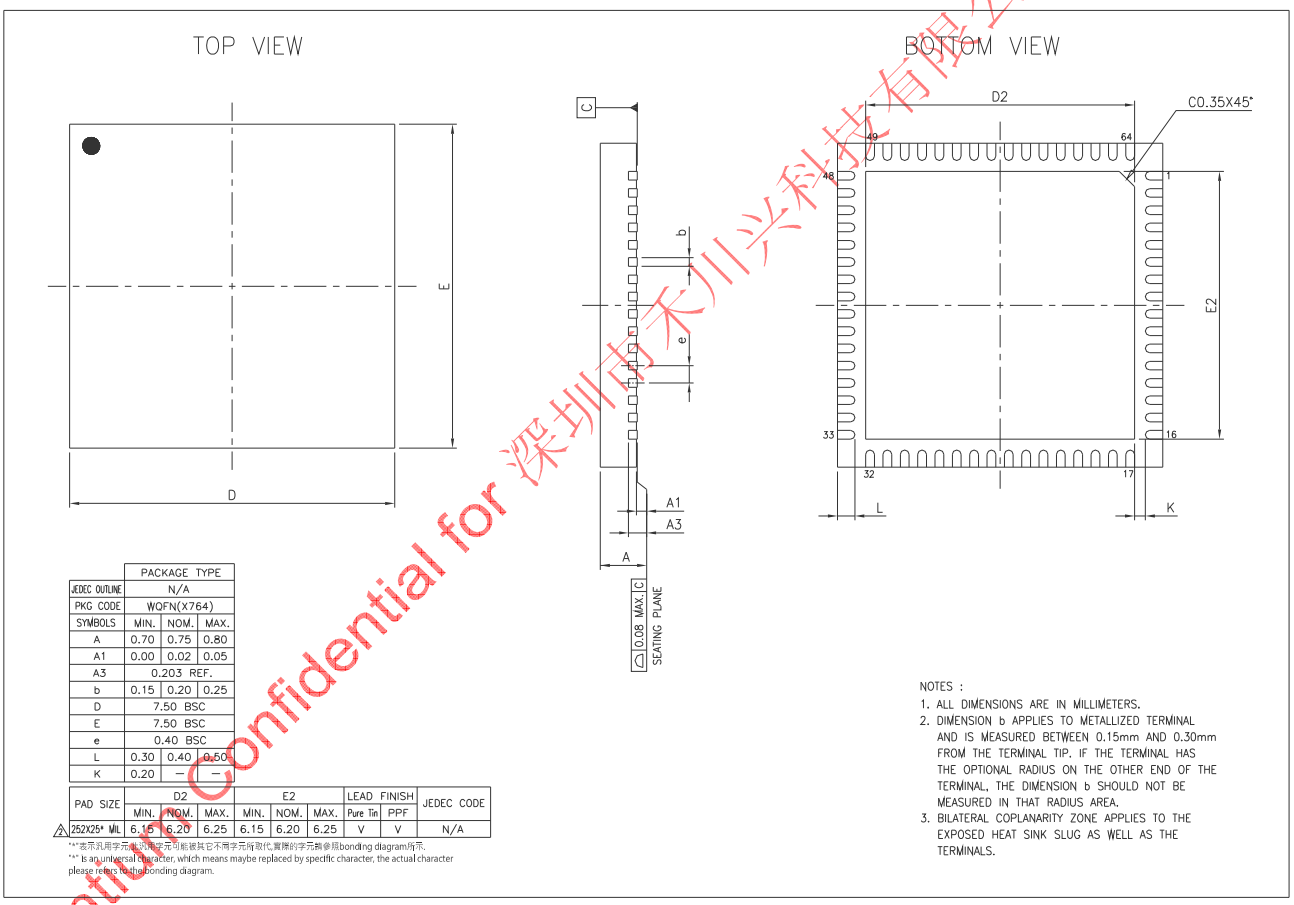
9.1 ePad Enhancement

The LT8711EH-C is packaged in a 64-lead QFN package with ePad.

The ePad needs to be soldered to the PCB. The information in the following paragraphs is provided for applications which solder the ePad to the PCB.

The ePad must not be electrically connected to any other voltage level except ground (GND). A clearance of at least 0.25mm should be designed on the PCB between the edge of the ePad and the inner edges of the lead pads to avoid any electrical shorts.

9.2 Package Dimensions



	PACKAGE TYPE		
JEDEC OUTLINE	N/A		
PKG CODE	WQFN(X764)		
SYMBOLS	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3	0.203 REF.		
b	0.15	0.20	0.25
D	7.50 BSC		
E	7.50 BSC		
e	0.40 BSC		
L	0.30	0.40	0.50
K	0.20	–	–

PAD SIZE	D2			E2			LEAD FINISH		JEDEC CODE
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	Pure Tin	PPF	
252X25* MIL	6.15	6.20	6.25	6.15	6.20	6.25	V	V	N/A

A is an universal character, which means maybe replaced by specific character, the actual character please refers to the bonding diagram.

Figure 9.2.1 Package Dimensions

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