VIA Labs, Inc.

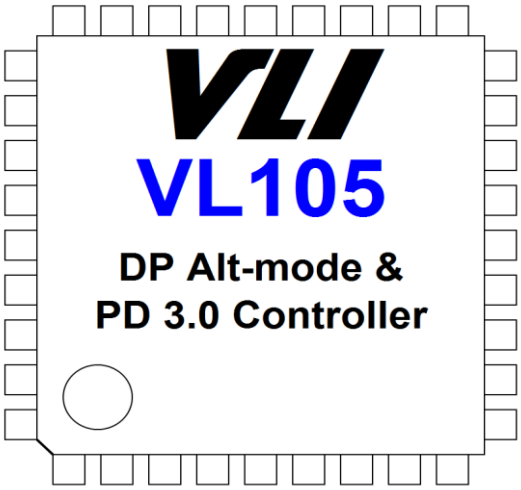
Datasheet

VL105

DP Alt-mode & PD 3.0 Controller For USB-C Devices

December 14th, 2018

Revision 1.00



Revision History

Rev	Date	Note	Initial
0.80	09/14/2018	Preliminary release	HC
1.00	12/14/2018	Remove the support of SCP/FCP Remove redundant USB Full Speed DC/AC Characteristics Remove built-in Ra and related spec Update Figure 1 by removing Vconn as power source Update Figure 3 by adding the support of Analog USB-C Audio Add Certification TID	HC

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Product Features

VL105

DisplayPort Alt-mode & PD 3.0 Controller for USB-C Devices

■**CC Logic & PD 3.0 Engine** supporting one charging UFP and two DRP DFPs
– Compliant to USB Type-C Cable and Connector Specification Revision 1.3
– Compliant to USB Power Delivery Specification Revision 3.0 Version 1.1
– Integrated Type-C transceivers, supporting one charging UFP and up to two DRP DFPs
– Built-in pull-up/pull down resistors, including Rp, Rd
– Built-in Vconn power switch

■**DP Alt-mode Configuration and SBU Switch**
– Compliant to VESA DisplayPort Alt Mode on USB Type-C Standard Version 1.0a
– DP mode Discovery/Enter/Exit; DP configure, status update, source/sink connection detection
– Built-in AUX/SBU switch for DP Alt-mode or USB-C analog audio

■**USB-C Charging UFP Capability**
– Charging connected PD hosts once external power is available
– Support Provider and Consumer roles
– Support PD Power Rule up to 100W
– Support dead battery charging and PD 3.0 Fast Role Swap

■**Two USB-C DRP DFPs Capability**
– Support Provider and Consumer roles
– Support PD Power Rule up to 100W as Sink and 15W as Source
– Either DFP port can charge host (as sink) by first-plugin-first-serve basis, the other port is then set to source mode only
– Built-in D+/D- Charging ePHY for chargers using D+/D- as protocol handshake

■**USB Interface and USB Billboard Device**
– USB Billboard compliant to USB Device Class Definition for Billboard Devices Revision 1.21
– Integrated in-house USB 2.0 Full-speed PHY
– Proprietary design for interchangeable charge through audio to select USB routing by first-plugin-first-serve basis

■**Fast 8051 Macro Cell 80C32-Compatible Microcontroller**
– Standard 1T 8051 instruction set with embedded Mask ROM and SRAM
– Support external SPI flash or sharing SPI flash with VLI Hub controller for firmware upgrade

■**Built-in Oscillator, Voltage Regulators, Voltage Detector, and Current Detector**
– Built-in trimmed RC oscillator
– 5.0V-to-3.3V LDO and 3.3V-to-1.8V LDO
– Vbus Voltage Detector and Vbus Current Detector for monitoring power safety

■**Smart Auto-standby**
– Automatically entering deep power saving mode when connected interface is in idle state

■**GPIOs for Special Function and Control**
– 15 GPIOs on QFN60 and 11 GPIOs on QFN48 for application customization and one I^2C master interface

■**Physical**
– QFN 60 green package (7x7x0.85 mm) for VL105-Q6
– QFN 48 green package (6x6x0.85 mm) for VL105-Q4 (pin compatible to VL103-Q4)

■**Certification**
– TID: 39, ID: 35048

■**Applications**
– USB-C charge through dongle or Multi-function dongle with any port charge through
– USB-C interchangeable charge through audio dongle

VL105 System Overview

VIA Lab's VL105 is a highly integrated single chip DisplayPort Alt-mode and Power Delivery 3.0 controller for USB-C devices designed for USB-C multi-function docks with charge through and interchangeable charge through audio dongles. Integrated USB-C charging UFP, VL105 can perform DP Alt-mode video output functionality and simultaneously charging connected PD host once external power is detected. Two integrated USB-C DRP DFPs can either connect to USB-C power adapter to charge PD host or connect to USB-C devices to access data transfer. D+/D- charging ePHY is integrated on both DRP DFPs to support chargers using D+/D- to do protocol handshake. Either DFP port can charge host by first-plugin-first-serve basis. VL105's Device Policy Manager could negotiate power rules between its DFP and UFP then enable power charge through. Charging a host under dead battery mode and PD 3.0 fast role swap are supported. A proprietary design for USB D+/D- routing is implemented by first-plugin-first-serve basis to support interchangeable charge through audio. SBU switch is built-in to support USB-C cable flipping feature and can support USB-C analog audio. USB Billboard device function is included to meet "VESA DP Alt-Mode on USB Type-C" spec. VL105 also support smart auto-standby that automatically entering deep power saving mode when connected interface is in idle state which is suitable for smart phone accessories.

Built-in trimmed RC oscillator, linear voltage regulators, Vbus voltage and current detectors, VL105 can work perfectly by Vbus power and monitor abnormal power behavior. Up to 15 GPIO pins are available for specific application usage. The SPI interface can support external SPI flash or sharing SPI flash with VLI Hub controller for firmware upgrade. VL105 is available in QFN 60L (7x7x0.85 mm) that supports two DRP DFPs. QFN 48L (6x6x0.85 mm) supports one DRP DFP and pin compatible to VL103-Q4.

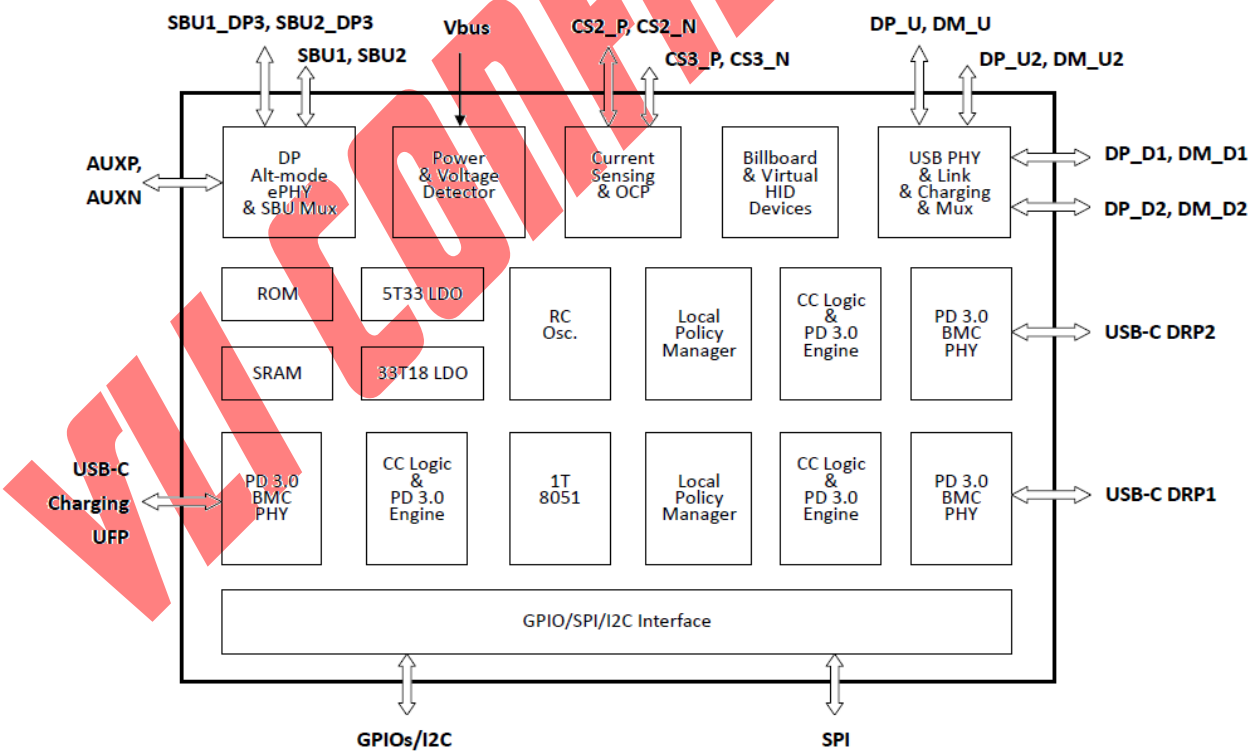


Figure 1 – VL105 Block Diagram

Typical Applications

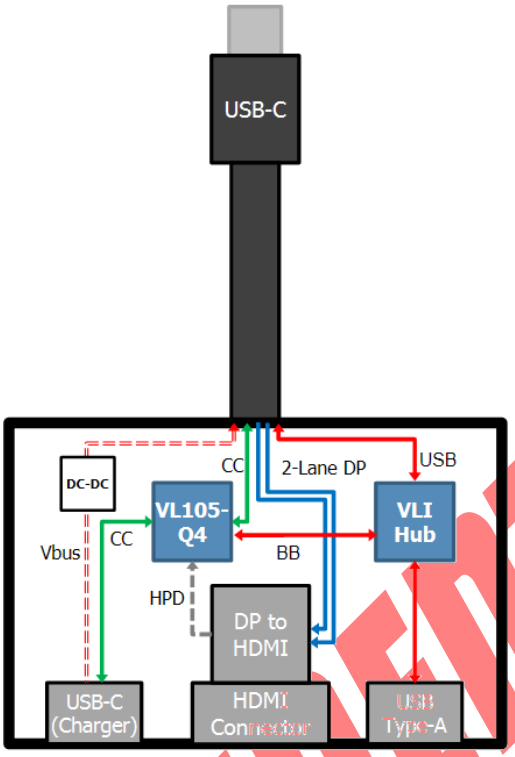


Figure 2 – Generic VL105-Q4 USB-C Multi-function Charge Through Dongle

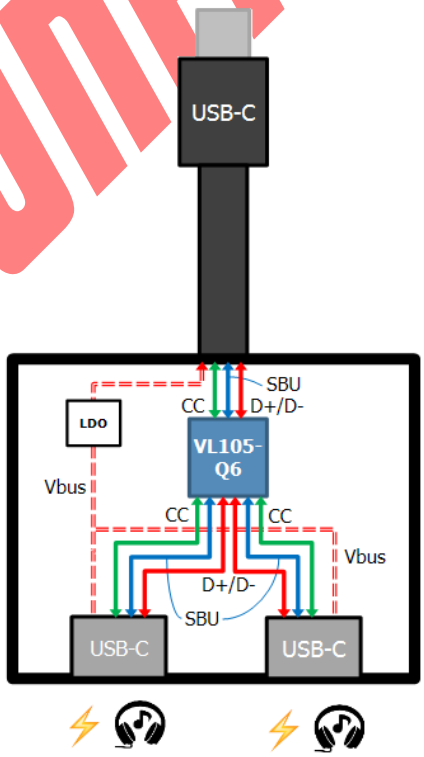


Figure 3 – VL105-Q6 USB-C Interchangeable Charge Through Audio Dongle

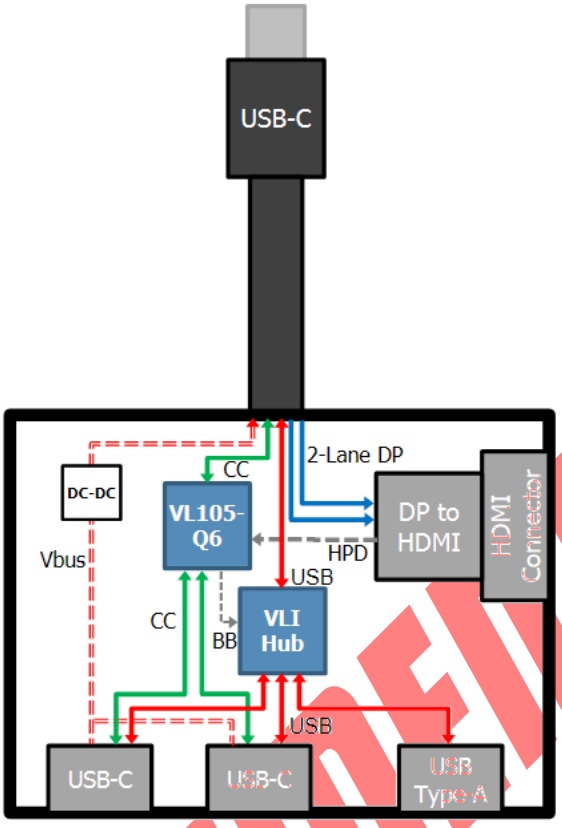


Figure 4 – Generic VL105-Q6 USB-C Multi-function Dongle with Any Port Charge Through

Pinout

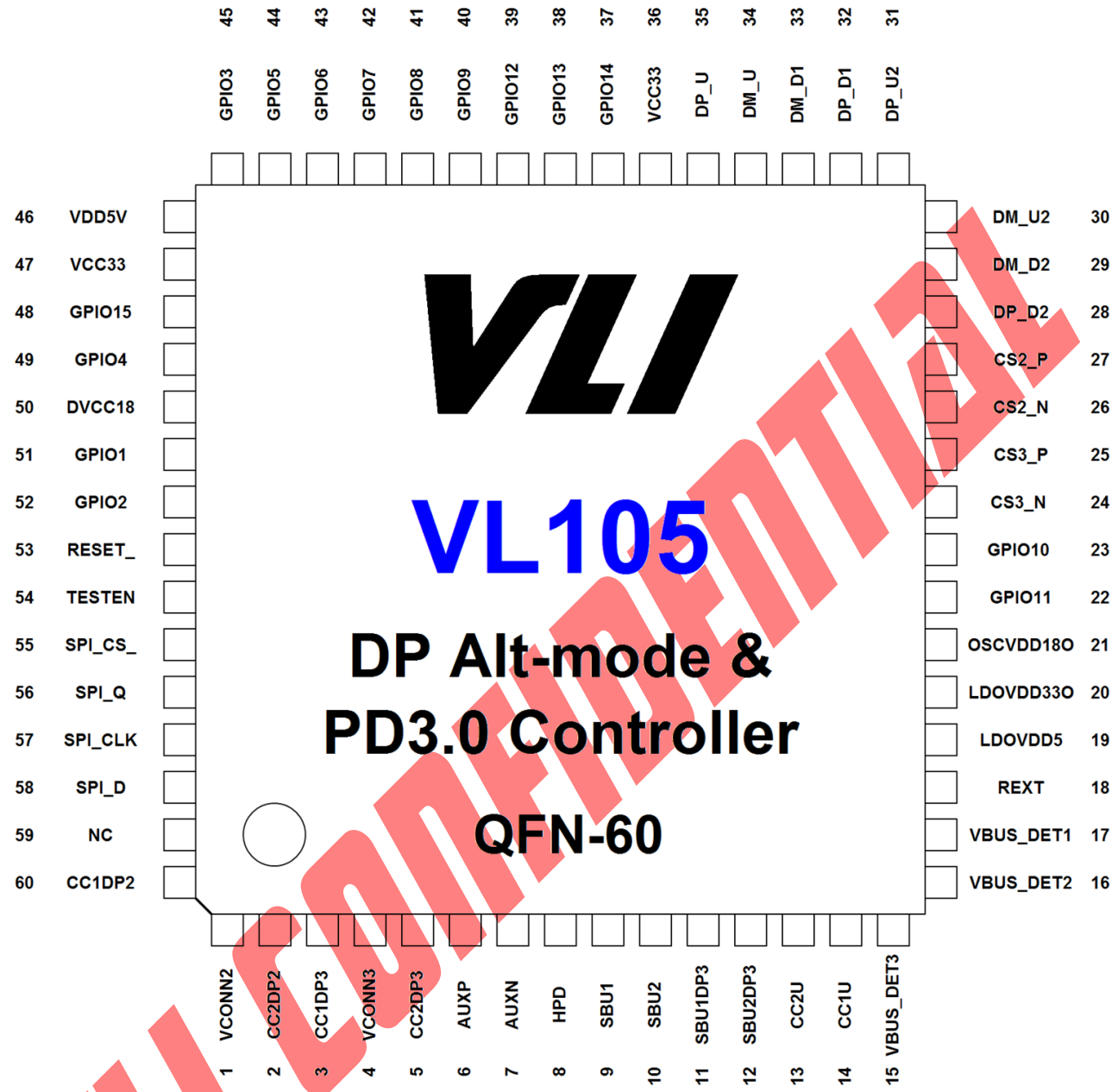


Figure 5 – VL105 QFN-60 Pin Diagram

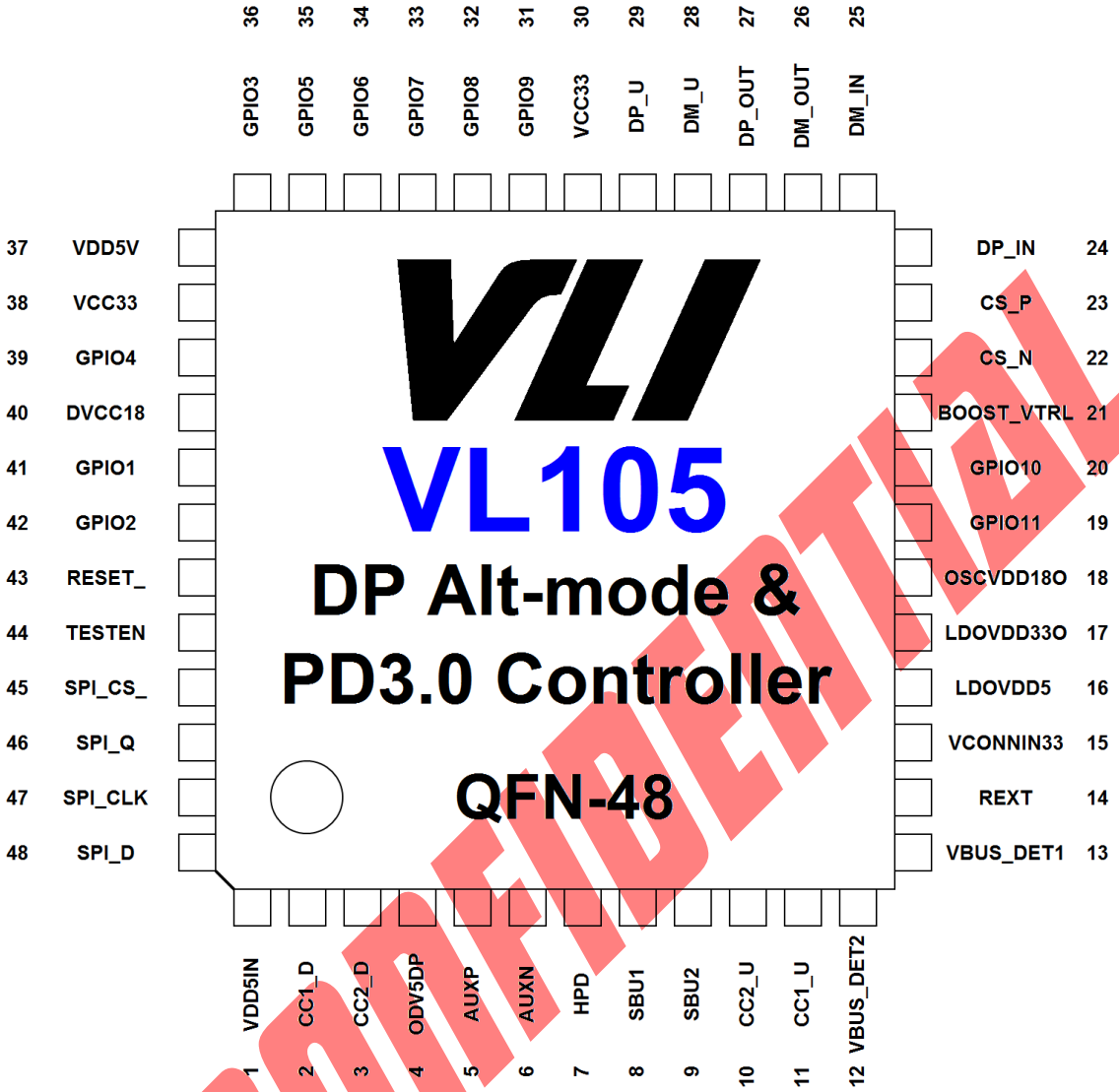


Figure 6 – VL105 QFN-48 Pin Diagram

Pin List

Table 1 – VL105 QFN-60 Pin List

Pin	Pin Name	Pin	Pin Name
1	VCONN2	31	DP_U2
2	CC2DP2	32	DP_D1
3	CC1DP3	33	DM_D1
4	VCONN3	34	DM_U
5	CC2DP3	35	DP_U
6	AUXP	36	VCC33
7	AUXN	37	GPIO14
8	HPD	38	GPIO13
9	SBU1	39	GPIO12
10	SBU2	40	GPIO9
11	SBU1DP3	41	GPIO8
12	SBU2DP3	42	GPIO7
13	CC2U	43	GPIO6
14	CC1U	44	GPIO5
15	VBUS_DET3	45	GPIO3
16	VBUS_DET2	46	VDD5V
17	VBUS_DET1	47	VCC33
18	REXT	48	GPIO15
19	LDOVDD5	49	GPIO4
20	LDOVDD33O	50	DVCC18
21	OSCVDD18O	51	GPIO1
22	GPIO11	52	GPIO2
23	GPIO10	53	RESET_
24	CS3_N	54	TESTEN
25	CS3_P	55	SPI_CS_
26	CS2_N	56	SPI_Q
27	CS2_P	57	SPI_CLK
28	DP_D2	58	SPI_D
29	DM_D2	59	NC
30	DM_U2	60	CC1DP2

Table 2 – VL105 QFN-48 Pin List

Pin	Pin Name	Pin	Pin Name
1	VDD5IN	25	DM_IN
2	CC1_D	26	DM_OUT
3	CC2_D	27	DP_OUT
4	ODV5DP	28	DM_U
5	AUXP	29	DP_U
6	AUXN	30	VCC33
7	HPD	31	GPIO9
8	SBU1	32	GPIO8
9	SBU2	33	GPIO7
10	CC2_U	34	GPIO6
11	CC1_U	35	GPIO5
12	VBUS_DET2	36	GPIO3
13	VBUS_DET1	37	VDD5V
14	REXT	38	VCC33
15	VCONNIN33	39	GPIO4
16	LDOVDD5	40	DVCC18
17	LDOVDD33O	41	GPIO1
18	OSCVDD18O	42	GPIO2
19	GPIO11	43	RESET_
20	GPIO10	44	TESTEN
21	BOOST_VTRL	45	SPI_CS_
22	CS_N	46	SPI_Q
23	CS_P	47	SPI_CLK
24	DP_IN	48	SPI_D

Pin Descriptions

Signal Type Definition

Name	Type	Signal Description
Input	I	A standard input-only signal
Output	O	A standard active driver
Input/ Output	I/O	A bi-directional signal
Analog bias	A_{BIAS}	Analog bias or reference signal. Must be tied to external resistor and/or capacitor bias network
Power	PWR	A power pin
Ground	GND	A ground pin

USB-C Interface

Pin Name	QFN60	QFN48	I/O	Signal Description
CC1_U (CC1U)	14	11	I/O	Charging UFP Configuration Channel 1
CC2_U (CC2U)	13	10	I/O	Charging UFP Configuration Channel 2
CC1_D (CC1DP2)	60	2	I/O	DRP DFP Port2 Configuration Channel 1
CC2_D (CC2DP2)	2	3	I/O	DRP DFP Port2 Configuration Channel 2
CC1DP3	3	—	I/O	DRP DFP Port3 Configuration Channel 1
CC2DP3	5	—	I/O	DRP DFP Port3 Configuration Channel 2
SBU1	9	8	I/O	Sideband Use 1
SBU2	10	9	I/O	Sideband Use 2
SBU1DP3	11	—	I/O	DRP DFP Port3 Sideband Use 1
SBU2DP3	12	—	I/O	DRP DFP Port3 Sideband Use 2

USB Interface & USB Billboard

Pin Name	QFN60	QFN48	I/O	Signal Description
DP_U	35	29	I/O	D+ Data Line to USB Billboard Device or Data Input
DM_U	34	28	I/O	D– Data Line to USB Billboard Device or Data Input
DP_IN (DP_D1)	32	24	I/O	D+ Data Line Connect to DFP Port2
DM_IN (DM_D1)	33	25	I/O	D– Data Line Connect to DFP Port2
DP_D2	28	—	I/O	D+ Data Line Connect to DFP Port3
DM_D2	29	—	I/O	D– Data Line Connect to DFP Port3
DP_OUT (DP_U2)	31	27	I/O	D+ Data Line Connect to Upstream Facing Port (to Hub)
DM_OUT (DM_U2)	30	26	I/O	D– Data Line Connect to Upstream Facing Port (to Hub)

DP Alt-mode Interface

Pin Name	QFN60	QFN48	I/O	Signal Description
AUXP	6	5	I/O	DP AUX Channel Positive (DRP DFP Port2 SBU1)
AUXN	7	6	I/O	DP AUX Channel Negative (DRP DFP Port2 SBU2)
HPD	8	7	I	DP Hot Plug Detect

SPI Interface

Pin Name	QFN60	QFN48	I/O	Signal Description
SPI_CS_	55	45	O	Serial Flash Chip Enable
SPI_D	58	48	O	Serial Flash Data Input
SPI_Q	56	46	I	Serial Flash Data Output
SPI_CLK	57	47	O	Serial Flash Clock

Analog Command Block

Pin Name	QFN60	QFN48	I/O	Signal Description
REXT	18	14	A_{BIAS}	Connect to External Resistor (243K ohm, +/- 1% accuracy)
LDOVDD5	19	16	PWR	5V Input for 5V-to-3.3V LDO
LDOVDD33O	20	17	PWR	3.3V Output Pin for 5V-to-3.3V LDO
OSCVDD18O	21	18	PWR	Analog 1.8V Power Output
VCONNIN33	—	15	PWR	Dummy Pin
VBUS_DET1	17	13	I	Charging UFP VBus Power Input for Removal Detection
VBUS_DET2	16	12	I	DRP DFP Port2 Vbus Power Input for Removal Detection
VBUS_DET3	15	—	I	DRP DFP Port3 Vbus Power Input for Removal Detection
CS_P (CS2_P)	27	23	I	DRP DFP Port2 Current Sensing Positive Input
CS_N (CS2_N)	26	22	I	DRP DFP Port2 Current Sensing Negative Input
CS3_P	25	—	I	DRP DFP Port3 Current Sensing Positive Input
CS3_N	24	—	I	DRP DFP Port3 Current Sensing Negative Input
BOOST_VTRL	—	21	I	Boost Voltage Control Input
VDD5IN (VCONN2)	1	1	PWR	5V Input Power for DRP DFP Port2 VCONN
VCONN3	4	—	PWR	5V Input Power for DRP DFP Port3 VCONN
ODV5DP	—	4	O	Open-Drain IO for 5V Video Power Control

Test Pin

Pin Name	QFN60	QFN48	I/O	Signal Description
TESTEN	54	44	I	Test Mode Enable; Internal pull down Do not connect for normal operation.

Power and Ground

Pin Name	QFN60	QFN48	I/O	Signal Description
VDD5V	46	37	PWR	E-fuse Power Input, Connecting to 3.3V in Normal Use
VCC33	36, 47	30, 38	PWR	Digital 3.3V IO Power
DVCC18	50	40	PWR	Digital 1.8V Core Power
VSS	EPAD	EPAD	GND	Ground

General Purpose I/O and Miscellaneous

Pin Name	QFN60	QFN48	I/O	Signal Description
RESET_	53	43	I	External Chip Reset
GPIO1	51	41	I/O	General Purpose I/O
GPIO2	52	42	I/O	General Purpose I/O
GPIO3	45	36	I/O	General Purpose I/O
GPIO4	49	39	I/O	General Purpose I/O
GPIO5	44	35	I/O	General Purpose I/O
GPIO6	43	34	I/O	General Purpose I/O
GPIO7	42	33	I/O	General Purpose I/O
GPIO8	41	32	I/O	General Purpose I/O
GPIO9	40	31	I/O	General Purpose I/O
GPIO10	23	20	I/O	General Purpose I/O
GPIO11	22	19	I/O	General Purpose I/O
GPIO12	39	—	I/O	General Purpose I/O
GPIO13	38	—	I/O	General Purpose I/O
GPIO14	37	—	I/O	General Purpose I/O
GPIO15	48	—	I/O	General Purpose I/O
NC	59	—	—	Not Connected

Electrical Specification

Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit	Note
T_{STG}	Storage Temperature	-55	125	°C	—
V_{DD33}	3.3V Power Input Voltage	-0.5	3.69	V	—
V_{DD50}	5V Power Input Voltage	-0.5	5.5	V	—
V_O	Output Voltage at any output	-0.5	VCC+ 0.5	V	—
V_{ESD}	Electrostatic Discharge	-2	2	kV	Human Body Model

Note:
1. Stress above conditions may cause permanent damage to the device. Functional operation of this device should be restricted to the conditions described.

Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
LDOVDD5	5V to 3.3V LDO 5V Power Input	4.5	5	5.5	V
VCC33	Digital IO power 3.3V	3.0	3.3	3.6	V
DVCC18	Digital Core power 1.8V	1.62	1.8	1.98	V
DGND	Ground	—	0	—	V
T_A	Ambient Temperature	0		70	°C

General IO DC Characteristics

Symbol	Parameter	Min	Max	Unit	Note
V_{IL}	Input Low Voltage	-0.30	0.8	V	—
V_{IH}	Input High Voltage	2.0	3.6	V	—
V_{OL}	Output Low Voltage	—	0.4	V	IOL=15.8mA
V_{OH}	Output High Voltage	2.4	—	V	IOH=26.5mA
I_{IL}	Input Leakage Current	—	+/-10	μA	0<VIN<VCC
I_{OZ}	Tristate Leakage Current	—	+/-10	μA	0<VOUT<VCC

Internal 3.3V to 1.8V LDO Regulator

Parameter	Min	Typ.	Max	Unit	Note
Input Voltage	3.0	3.3	3.6	V	
Output Voltage	1.71	1.8	1.89	V	
Max. Output Current			100	mA	

Internal 5V to 3.3V LDO Regulator

Parameter	Min	Typ.	Max	Unit	Note
Input Voltage	4.5	5.0	5.5	V	
Output Voltage	3.135	3.3	3.465	V	
Max. Output Current			100	mA	

PD BMC DC/AC Characteristics

Symbol	Parameter	Min	Max	Unit	Note
$V_{BMCSWING}$	Voltage Swing	1.05	1.2	V	—
Z_{BMCDRV}	Drive Output Resistance	33	75	Ω	—
T_{BMCR}	Rise Time	300		ns	—
T_{BMCF}	Fall Time	300		ns	—

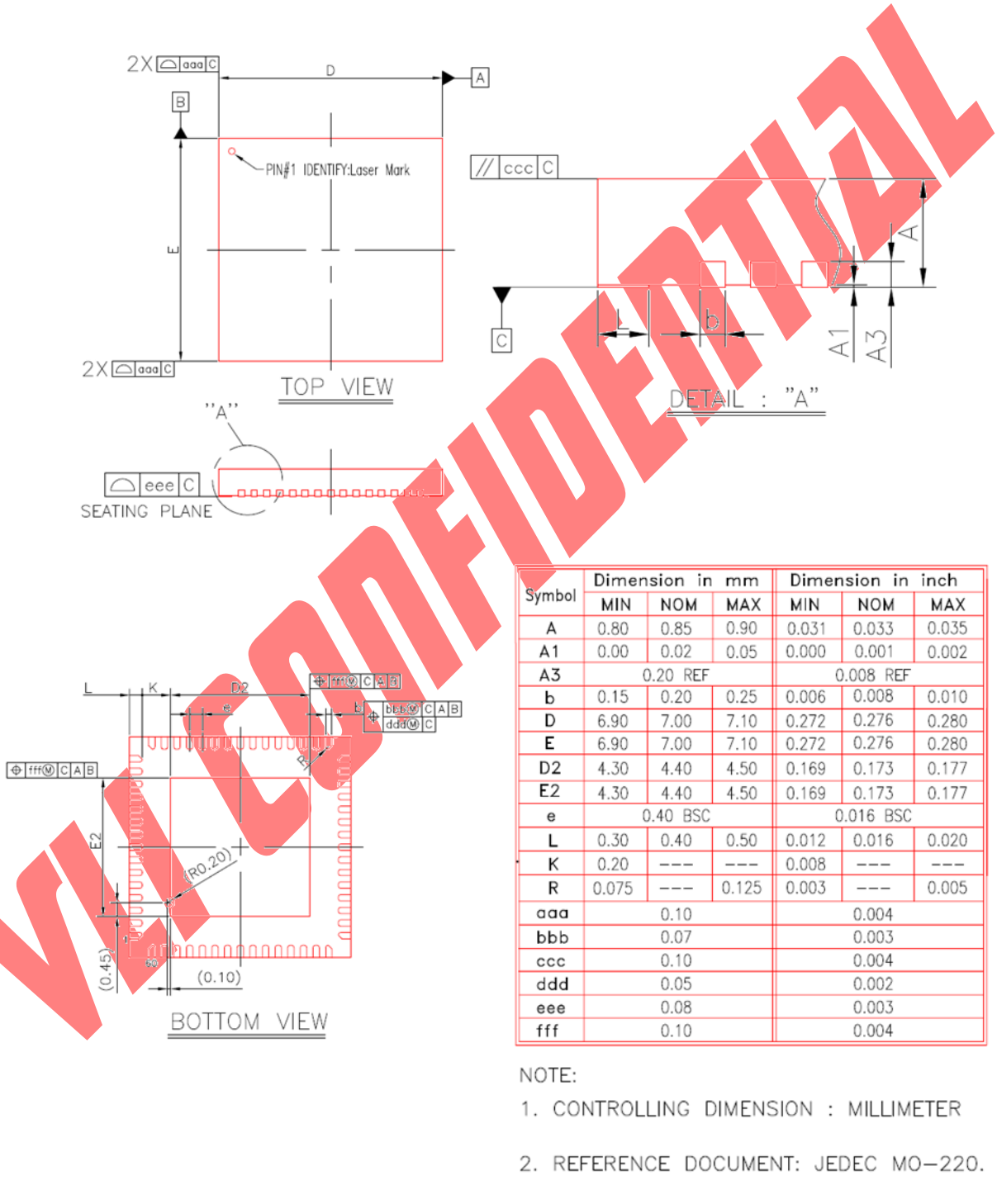
USB Full Speed DC/AC Characteristics

Symbol	Parameter	Min	Max	Unit	Note
V_{IH}	High state input level	2.0		V	—
V_{IHZ}	High-z state input level	2.7	3.6	V	—
V_{IL}	Low state input level		0.8	V	—
V_{DI}	Differential input sensitivity	0.2		V	—
V_{CM}	Differential common mode	0.8	2.5	V	—
V_{OL}	Low state output level	0.0	0.3	V	—
V_{OH}	High state output level	2.8	3.6	V	—
V_{CRS}	Output signal crossover voltage	1.3	2.0	V	—
R_{PU}	Bus pull-up resistor	1.425	1.575	KΩ	—
Z_{DRV}	Driver output resistance	28	44	Ω	—
T_{FR}	Full-speed Rise Time	4	20	ns	—
T_{FF}	Full-speed Fall Time	4	20	ns	—

Package Mechanical Specifications

QFN-60 Pb-free Maximum Temperature for IR Reflow

Parameter	Value	Unit
Maximum Temperature Tp	250	°C
Max Time within 5°C of Tp	30	seconds



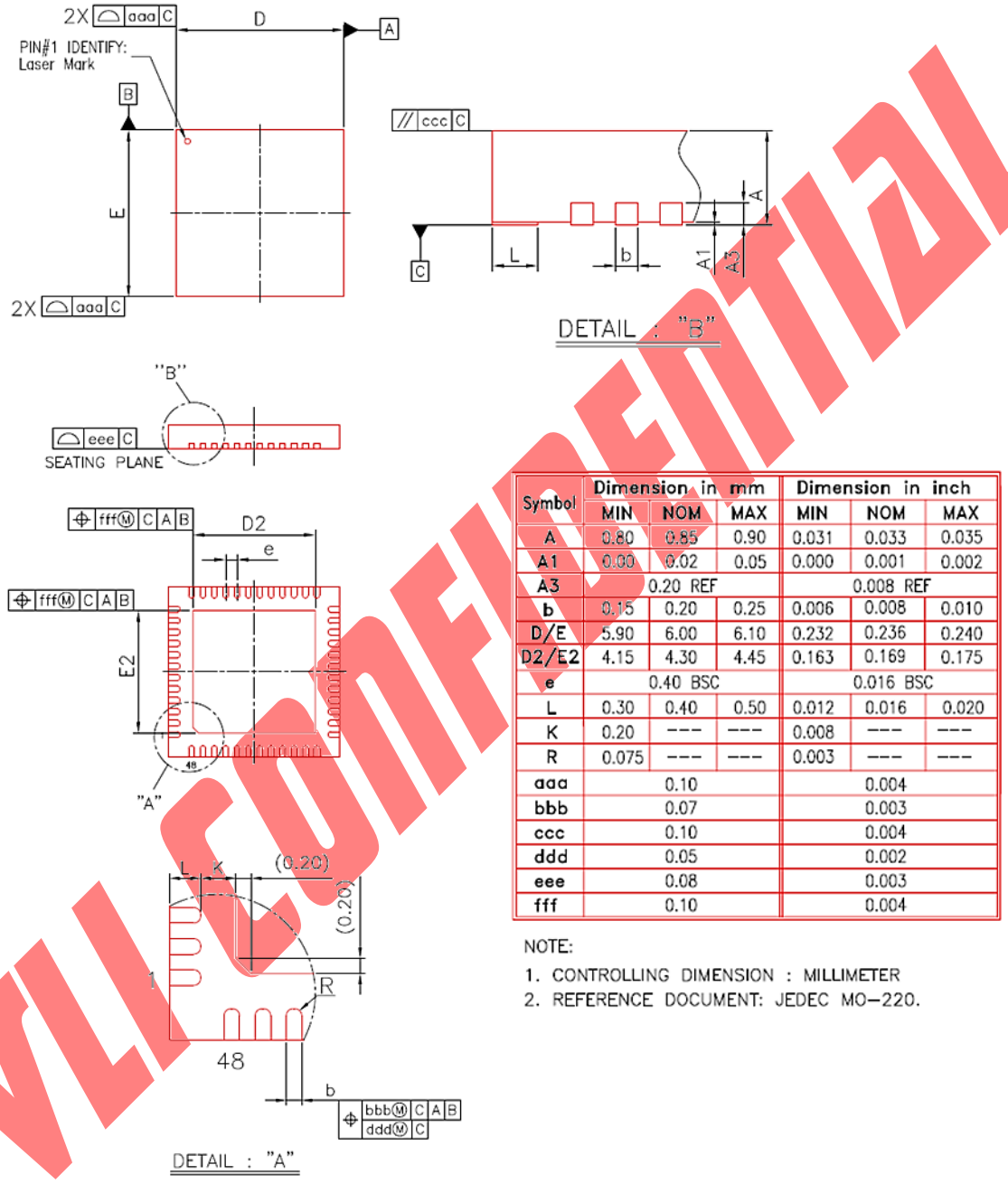
Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.80	0.85	0.90	0.031	0.033	0.035
A1	0.00	0.02	0.05	0.000	0.001	0.002
A3		0.20 REF			0.008 REF	
b	0.15	0.20	0.25	0.006	0.008	0.010
D	6.90	7.00	7.10	0.272	0.276	0.280
E	6.90	7.00	7.10	0.272	0.276	0.280
D2	4.30	4.40	4.50	0.169	0.173	0.177
E2	4.30	4.40	4.50	0.169	0.173	0.177
e		0.40 BSC			0.016 BSC	
L	0.30	0.40	0.50	0.012	0.016	0.020
K	0.20	---	---	0.008	---	---
R	0.075	---	0.125	0.003	---	0.005
aaa		0.10			0.004	
bbb		0.07			0.003	
ccc		0.10			0.004	
ddd		0.05			0.002	
eee		0.08			0.003	
fff		0.10			0.004	

NOTE:
1. CONTROLLING DIMENSION : MILLIMETER
2. REFERENCE DOCUMENT: JEDEC MO-220.

Figure 7 – QFN 60L 7x7x0.85 mm Mechanical Specification

QFN-48 Pb-free Maximum Temperature for IR Reflow

Parameter	Value	Unit
Maximum Temperature Tp	250	°C
Max Time within 5°C of Tp	30	seconds



Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.80	0.85	0.90	0.031	0.033	0.035
A1	0.00	0.02	0.05	0.000	0.001	0.002
A3	0.20 REF			0.008 REF		
b	0.15	0.20	0.25	0.006	0.008	0.010
D/E	5.90	6.00	6.10	0.232	0.236	0.240
D2/E2	4.15	4.30	4.45	0.163	0.169	0.175
e	0.40 BSC			0.016 BSC		
L	0.30	0.40	0.50	0.012	0.016	0.020
K	0.20	---	---	0.008	---	---
R	0.075	---	---	0.003	---	---
aaa	0.10			0.004		
bbb	0.07			0.003		
ccc	0.10			0.004		
ddd	0.05			0.002		
eee	0.08			0.003		
fff	0.10			0.004		

NOTE:
1. CONTROLLING DIMENSION : MILLIMETER
2. REFERENCE DOCUMENT: JEDEC MO-220.

Figure 8 – QFN 48L 6x6x0.85 mm Mechanical Specification

Package Top Side Marking

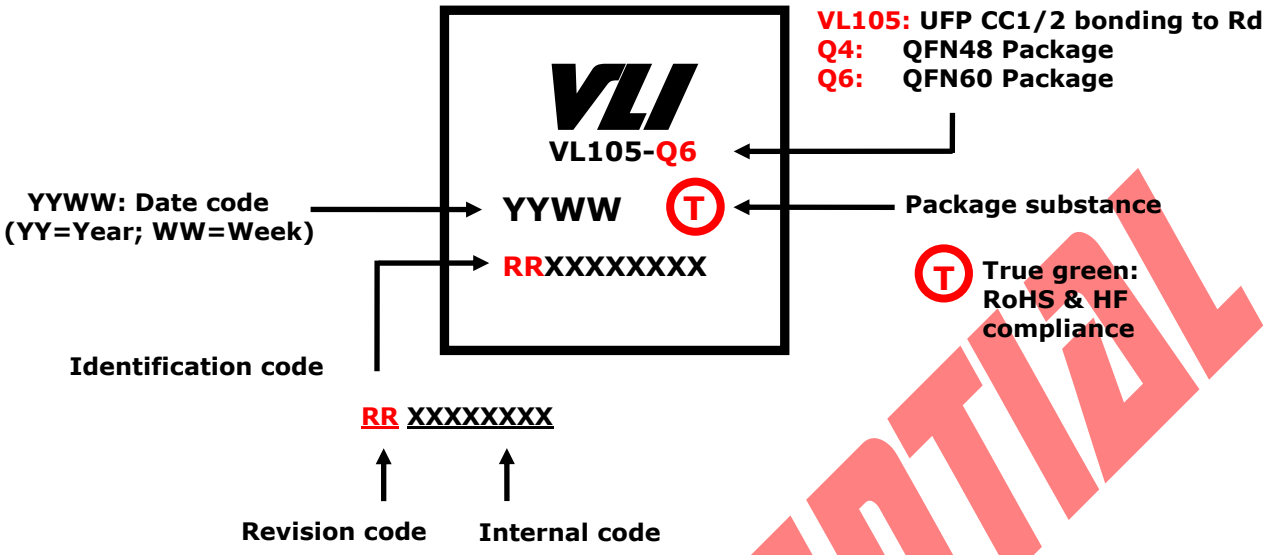


Figure 9 – VL105 QFN Package Top Side Marking

Ordering Information

Please contact VIA Labs sales representative or distributor in your region for ordering part number details.

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